UNIVERSITY OF NAIROBI

DESIGN OF INVERTER DRIVE FOR SYNCHRONOUS MOTORS

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BY

MAUKA N. CHRISTINE
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SUPERVISOR: MR. OGABA

EXAMINER: DR ABUNGU

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DEDICATION

To my lovely parents, brothers and sisters

ACKNOWLEDGEMENT

My greatest regards go to the highest God who gave me life and strength to do this project successfully. He deserves all the glory and honor.

I thank my family for the support they gave to me both financially and through encouragement in my entire academic life and especially in this project.

My special thanks also go to my supervisor for the genuine support that he gave me; he took his time to challenge me in the areas that called for keen interest over my project.

Finally, I thank some of my classmates and friends who supported me with constructive ideas over my project and encouraged me to move on.

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ABSTRACT

The growth in a high volume market in the variable speed drives is due the emerging applications in home appliances, HVAC drive, professional hand tools, automobile accessories, fans, pumps and process drives. The inverter-controlled synchronous motor is best suited for such applications because of the following:

- It is possible to vary the output voltage of the motor and thus different load with different voltage requirements can be operated
- The power factor of the motor can be easily changed thus suiting different applications
- The frequency and thus the speed of the motor can varied

This project addresses the design and development of a variable-voltage variable-frequency inverter drive for a synchronous motor. The issues addressed in this paper include the design specifications, design of ac to dc converter, design of gate firing circuit, commutation circuits, inverter and LC filters. The results from both the simulations and the experimental inverter are presented to correlate the key design aspects and design specifications.

1. INTRODUCTION

A synchronous motor is a constant speed machine, that is, the speed of the motor does not change with the load. This is because the speed of the motor depends on the supply frequency. Due to emerging need for variable speed and hence output frequency, the variable-voltage-variable frequency speed drives are required.

The objectives of this project are: to survey the of operation of synchronous machine, to design an inverter source to control the following parameters of the synchronous motor: 3 phase voltage magnitude and frequency (variable below and above the normal value-50 Hz) and implement the designed inverter on the existing synchronous motor.

The paper is organized as follows: Chapter 2 outlines the theory of the operation of a synchronous motor. The variable speed drives are presented in chapter3. Chapter4 presents the drive system configuration in a schematic form where the subsystems are functionally identified. The design of various subsystems and their realization are given in Chapter **5**. Experimental results from the prototype inverter fed induction motor drive are presented in chapter 6 to validate the design and conformity to specifications. Finally, conclusions presented in chapter 7.

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2. OPERATION OF SYNCHRONOUS MOTORS

Three phase synchronous machines operated as generators mostly generate three-phase power. The synchronous motors are utilized in industrial applications that require constant speed rotation.

A synchronous motor is a constant speed machine, which always rotates with zero speed at a synchronous speed, which is dependent on frequency and the number of poles.

The synchronous motors consist of two parts namely; a rotor, which is the rotating part, and a stator, which is a stationary, part with a central cavity to accommodate the rotor.

The motor has the following characteristics:

i. It runs either at synchronous speed or not at all, that is, while running it maintains a constant speed. The only way to change its speed is to vary the supply frequency since the speed of the motor is given by equation(1)

$$Ns = 120f/p \qquad (1.1)$$

From equation (1), the speed (*Ns*) of the motor can be controlled by either adjusting the supply frequency (f) or the number of poles (p.).

ii. It is not inherently self –starting. It has to run up to synchronous speed by some means before synchronization to the supply.

iii. It is capable of being operated under a wide range of power factors both lagging and leading.

Synchronous motors have a poly phase winding on the stator also known as the armature and a field winding carrying a dc current on the rotor. There are two types of magneto motive forces involved, one due to field current and the other due armature current. The armature current is identical to the stator of induction motors but there is no induction in the rotor.

2.1 Types of synchronous motors

Synchronous motors are classified as

i. Cylindrical rotor motors
ii. Salient pole motors
iii. Reluctance motors
iv. switched reluctance motors
v. permanent magnet motors
vi. brushless dc and ac motors

2.2 Cylindrical rotor motors

These were available in the machines laboratory at time of the project, hence, there theory was the only one considered.

The field winding is wound on the rotor that is cylindrical in nature and these motor have uniform air gap. The motor reactance is independent of the rotor position. The equivalent circuit and phasor diagrams of the motor are as shown in the figures 1.1 and 1.2 respectively.

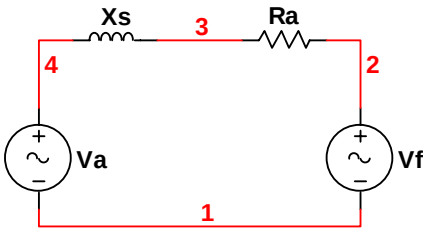


Fig.1.1 Equivalent circuit diagram of the motor

Where Xs=synchronous reactance per phase

Ra=armature resistance per phase

VF=excitation (field) voltage-dependent on field

Va =armature voltage

δ

0 Va

$-jXsIa$

$\boldsymbol{\phi}$m If Vf

Fig.1.2 The phasor diagram of the synchronous motor

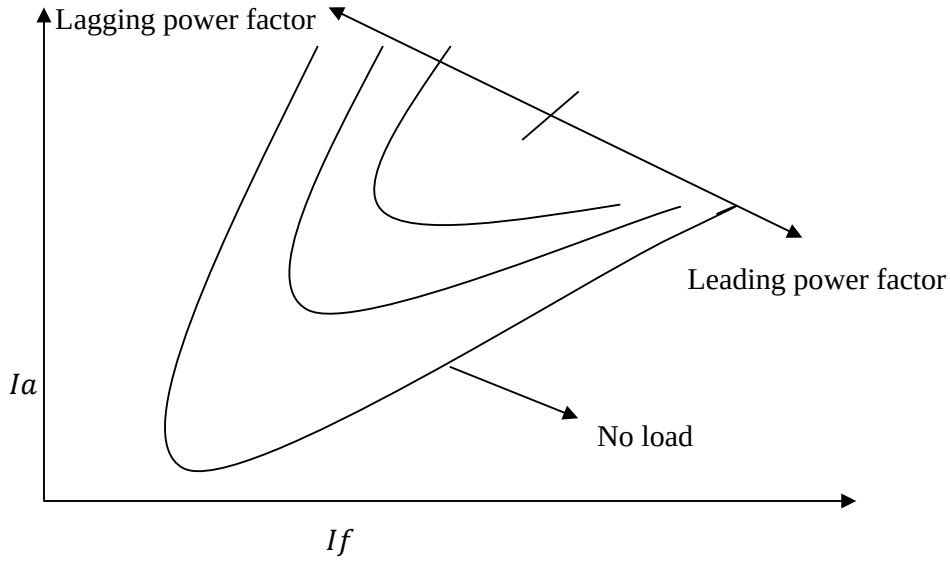


Fig.1.3 V curves for synchronous motor

Ia= Armature current

If=Field current

From figure1.2, it is clear that the power factor depends on the field current, If

If $\boldsymbol{\phi}$m is the lagging Power factor of the motor, then

$$VF = Va \ < 0° - Ia\ (Ra + jXs) \qquad (1.2)$$

$$= Va < 0 - Ia\ (cos\ \phi m - jsin\phi m) \times (Ra + jXs)$$

$$= Va - IaXs \times sin\phi m - IaRa \times cos\phi m - jIa\ (Xscos\phi m - RaSin\phi m)$$

$$= vf < k$$

Where k=$arc\ Tan - \{(IaXscos\phi m - IaRasin\phi m)/\ (Va - IaXsSin\phi m - IaRacos\phi m)\}$

$vf = \{(VCa - IaXsSin\phi m - IaRaCos\phi m)$ ^2 + $(IaXsCos\phi m - IaRaSin\phi m)$^2}^0.5

The phasor diagram Yields;

$$Ia = VF/Ra - VF/jXs \qquad (1.3)$$

$$= [Va - vf\ (cosk + jsink) \times (Ra - jXs)/\ (Ra\text{^}2 + Xs\text{^}2)$$

The power input to the motor is,

$$Pi = 3VaIa \cos \phi m \qquad (1.4)$$

$$= 3(Ra\ [VA\text{^}2 - Vavfcosk] - [VavfXssink])\ (/Ra\text{^}2 + Xs\text{^}2)$$

The stator copper loss is,

$$Psu = 3Ia\text{^}2 \times Ra \qquad (1.5)$$

$$The\ gap\ power\ = Power\ developed = Pd = Pg = Pi - Psu$$

If ωs is the synchronous speed, which is the same as the rotor speed, then the developed torque is,

$$Td = Pd/\omega s \tag{1.6}$$

If the armature resistance is negligible then

$$Td = -3Vavf \sin k\ /Xs\omega s \tag{1.7}$$

Where

k=-$\tan^{-1}(IaXs \cos \phi m\ /Va - IaXs \sin \phi m)$

For motoring, k is negative and torque is positive. Incase k is positive, both the power and the torque are negative. For fixed voltage and frequency, torque depends on angle k and is proportional to excitation voltage. For fixed value of vf and k, torque depends on voltage to frequency ratio and a constant voltage per hertz control will produce speed control at a constant torque. If Va, Vf and k remain constant, the torque decreases with speed and the motor operates on the field weakening mode. If $k = 90°$, the torque becomes maximum and it is called pullout torque which is

$$Tp = Tm = -3Vavf/Xs\omega s \tag{1.8}$$

The torque versus torque angle characteristic for the cylindrical rotor motor is as shown in figure1.4

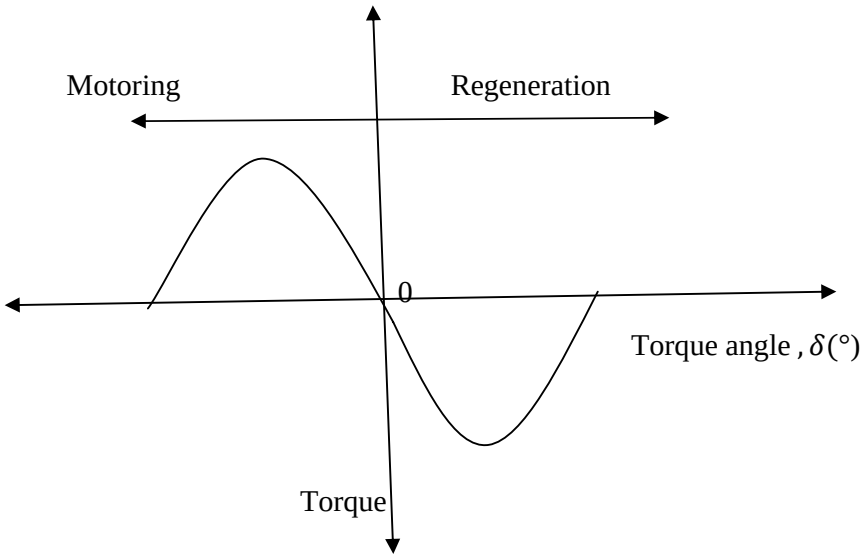


Fig.1.4 The torque versus angle characteristics

3. VARIABLE- FREQUENCY SYNCHRONOUS MACHINE DRIVES

Variable speed drives are required for the following reasons

- Match the speed of a drive to the process requirements
- Match the torque of a drive to the process requirements
- Save energy and improve efficiency

The speed of a synchronous motor is varied by changing the stator supply frequency. AC drives that use a PWM type schemes have varying levels of performance based on control algorithms. There are four basic types of control for AC drives today. These are Volts per Hertz, Sensor less Vector Control, Flux Vector Control, and Field Oriented Control.

V/Hz control is a basic control method, providing a variable frequency drive for applications like fan and pump. It provides fair speed and torque control, at a reasonable cost.

Sensor less Vector control provides better speed regulation, and the ability to produce high starting torque

Flux Vector control provides more precise speed and torque control, with dynamic response.

Field Oriented Control drives provide the best speed and torque control available for AC motors. It provides DC performance for AC motors, and is well suited for typical DC applications.

3.1.1 Open loop frequency control

An independent oscillator determines the speed of the motor and the stator voltage is directly controlled.

3.1.2.Closed loop or self –synchronous control

The stator voltage can be controlled directly by the varying the stator frequency .For example by a signal obtained from a rotor shaft sensor (these signals are used as firing signals for thyristor gates). The inverter output supplies the three- phase ac motor. In this case, by monitoring the rotor position, the magnetic axis of the field winding is determined and since these signals are used for firing the gates of the SCRs of the inverter, as a dc machine, a fixed space angle can be maintained between the field winding and the stator magneto motive force. It is also possible to use terminal voltages of motor for synchronization of the firing signals of the inverter.

3.2 Types of inverters

i. Voltage fed inverter (VFI) where the input voltage remains constant
ii. Current fed inverter (CFI) where the input current remains constant
iii. Variable dc link inverter where the input voltage is controlled

3.2.1 Voltage fed Inverter

There are two types;

- Pulse Width modulated inverters (PWM*)* where an uncontrolled rectifier is used
- Square wave inverters; a controlled rectifier is used. However, the controlled rectifiers suffer from the following disadvantages; have low power factor at low voltage. They suffer from lagging power factor on ac Supply

3.2.2 Variable Voltage Inverter (VVI)

The variable voltage inverter (VVI) uses an SCR converter bridge to convert the incoming AC voltage into DC. The SCRs provide a means of controlling the value of the rectified DC voltage from zero to approximately 600 VDC. The L1 choke and
C1 capacitor(s) make up the DC link section and smooth the converted dc voltage.

The inverter section consists of six switching devices; switching devices include thyristors, bipolar transistors, MOSFETS, and IGBTs. The control logic uses a microprocessor or logic circuits to switch the transistors on and off providing a variable voltage and frequency to the motor. The motor prefers a smooth sine wave; a six-step output is satisfactorily used. The main disadvantage is torque pulsation, which occurs each time a switching device, such as a bipolar, is switched ON. The pulsations can be noticeable at low speeds as speed variations in the motor. These speed variations are referred to as cogging. The non-sinusoidal current waveform causes extra heating in the motor requiring a motor de-rating.

3.2.3 Current Source Inverter

The current source inverter (CSI) uses an SCR input to produce a variable voltage DC link. The inverter section also uses SCRs for switching the output to the motor. The current source inverter controls the current in the motor. The motor must be carefully matched to the drive current spikes, caused by switching. At low speeds, the current pulse causes the motor to cog.

3.3 Pulse Width Modulation

Pulse width modulation (PWM) drives provide a more sinusoidal current output to control frequency and voltage supplied to an AC motor. PWM drives are more efficient and typically provide higher levels of performance. A basic PWM drive consists of a converter, DC link, control logic, and an inverter. These subsections are as shown in figure3.1.

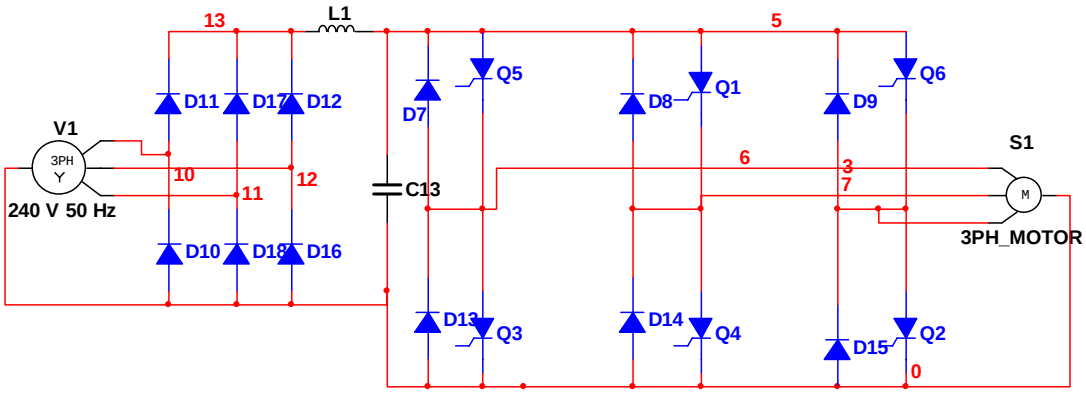


Fig.3.1 Inverter based on SCRs

3.3.1Converter and DC Link

Converter is the general term referring to a combination of rectifier and inverter circuits. However, the word commonly refers to rectifiers. The rectifier converts ac power to dc power. For the controlled rectifiers, SCRs are used and for the uncontrolled rectifiers, diodes are used.

The converter section consists of a fixed diode bridge rectifier, which converts the three-phase power supply to a DC voltage. The rectified DC value is approximately 1.35 times the line-to-line value of the supply voltage. The rectified DC value is approximately 149VDC for a 110 VAC supply.

The DC Link consists of low pass filter with an inductor, Lf and an electrolytic capacitorCf. The capacitor Cf limits voltage fluctuations at the input of the inverter. The inductor Lf assists the filter capacitor to maintain smooth dc link voltage and limits the ripples. Generally, the dc link ensures constant dc supply to the inverter.

3.3.2 Control Logic and Inverter

The inverter converts dc power to ac power. Inverters change a dc input voltage to a symmetrical input ac voltage of desired magnitude and frequency. A variable output voltage is obtained by varying the input dc voltage and maintaining the gain of the inverter constant. If the dc input voltage is constant, a variable output voltage is obtained by varying the gain of the inverter; normally accomplished by PWM control within the inverter.

The output should be ideally sinusoidal, but practical inverters produce non-sinusoidal waveforms and contain harmonics. In low and medium power applications, square-wave or quasi-square wave voltages may be used. In high power applications, low distorted sinusoidal waveforms are required. High power three phase outputs are 120/208v at 60Hz, 220/380v at 50Hz and 115/200v at 400Hz

The output voltage and frequency to the motor are controlled by the control logic and inverter section.

3.3.3 Switching devices

Several devices could be used to switch in the inverter. These include thyristors, insulated gate bipolar transistor, bipolar transistor and MOSFETS. The choice of the type of switching device depends on switching frequency required.

IGBTs

IGBTs (insulated gate bipolar transistor) provide a high switching speed necessary for PWM inverter operation. IGBTs are capable of switching on and off several thousand times a second. An IGBT can turn on in less than 400 nanoseconds and off in approximately 500 nanoseconds. An IGBT consists of a gate, collector and an emitter. When a positive voltage (typically +15 VDC) is applied to the gate, the IGBT will turn on. This is similar to closing a switch. Current will flow between the collector and emitter. An IGBT is turned off by removing the positive voltage from the gate. During the off state the IGBT gate voltage is normally held at a small negative voltage (-15 VDC) to prevent the device from turning on.

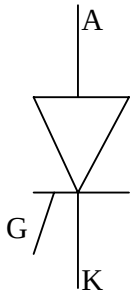
Thyristors

The word thyristor refers to a family name of solid-state devices designed for electronics switching and control of ac and dc power systems. Figure 5 shows the symbol for the thyristor. The symbols A, K and G stand for anode, cathode and gate respectively. The gate currents $I_{G,}$ depend on the type of SCR and rating of the anode current for example C106D has the following rating

$Vpiv$=400V

$I_{A=}$3.2A

I_G=0.2mA at V_G=1.2V



3.4 PWM Voltage and Current

More sinusoidal current output produced by the PWM reduces the torque pulsations, low speed motor cogging, and motor losses noticeable when using a six-step output. The voltage and frequency is controlled electronically by the circuitry within the AC drive. The fixed DC voltage (149 VDC) is modulated with this method to provide a variable voltage and frequency. At low output frequencies a low output voltage is required. The switching devices are turned on for shorter periods. Voltage and current build up in the motor is low. At high output frequencies a high voltage is required. The switching devices turn ON for longer periods, allowing voltage and current to build up to higher levels in the motor.

3.5. Commutation

. The thyristors require the reduction of load current to approximately zero to regain the ability to block the voltage in the forward direction. An external means is required in the circuits to do this if the current does not naturally approach zero or attempt to reverse.

3.5.1 Factors affecting commutation Turn-Off Time

The turn-off time is dependent on temperature and on forward and reverse current. Forward current is dictated by application under consideration, but in majority of the cases, the rate of rise and magnitude of reverse sweep-out current can be controlled by the circuit designer. The required turn-off time can be decreased through the design off commutation circuit.

In high frequency applications, the inductance is minimized to speed up the rise of reverse current .The magnitude should be limited to approximately 30A due to abrupt recovery of the reverse blocking junctions. The dissipation during turn-off however small also contributes to the losses of the device. The combination of turn-off times and power losses during these intervals affects the allowable output.

There are two methods commonly used for commutation in inverters, these are complimentary commutation and auxiliary commutation. In this paper, only the former is considered.

3.5.2 **Complimentary commutation**

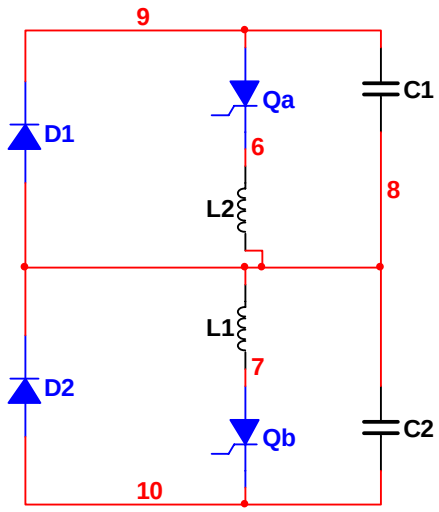


Fig. 3.3 The Mc Murray-Bedford inverter

If two inductors are tightly coupled, firing of one thyristor turns- off another thyristor in the other arm. The circuit operation can be divided into three modes as follows with assumptions that load currents remain constant during the commutating periods.

Mode1

This mode begins when Qa is fired to turn off Qb which was conducting. At the start, C2 is charged to Vs.C1 was shorted previously by $C2$ and has a voltage V_{L2}=Vs and L2 induces a voltage V_{L1}=Vs across L1. A reverse voltage of

$$Vak = Vs - VL1 - VL2 = -Vs \qquad (3.1)$$

is applied across T1 and forward current of T1 is forced to zero. Thus t_{off} (max) is dependent on load current Im and will be maximum when $Im = 0$.The maximum value of t-off is given by;

$$t(off)max = \frac{\pi}{3(\sqrt{2LmCm})} \qquad (3.2)$$

The available turn-off time can be determined from the condition that

V_{AK} (t) =0 in equation (9) giving

$$t - off = \sqrt{2LmCm}\,[1/\cos^{-1}\frac{1}{2\sqrt{(1+x^2)}} - \tan^{-1}x] \qquad (3.3)$$

Where x=$\frac{Im}{Vd}\sqrt{(\frac{2Lm}{Cm})}$

Mode2

This mode begins when diode d2 starts conducting. The energy stored in the inductor L2 is lost in the circuit formed by $Q2$, d2 and L2. The load current $iL\ (t)\ = Im$ also flows through diode d2 and thyristor $T2$; instantaneous current I_2 (t) for mode 2 is given by

$$Lm\frac{di2}{dt} + Vd = 0 \qquad (3.4)$$

With initial condition i_2 (t=0) $= Ip$, the solution is

$$t_2(t) = Ip - \frac{Lm}{Cm}\,t \qquad (3.5)$$

This mode ends when i2 (t) falls to zero and Qb is turned off due to self-commutation. The duration of this mode is

$$t_{2m} = IpLm/Vd \qquad (3.6)$$

Mode3

This mode begins when Q2 turns off. The diode d2 continues to carry load current until the load current falls to zero. Reverse bias voltage for Qb is provided by forward drop of diode d2.

4. THE SYSTEM SPECIFICATION AND DRIVE SYSTEM SCHEMATIC

The motor considered was rated 2KVA, the stator voltages and stator currents are 110V and 10.5A respectively, speed of 1500rpm, 3 phases at 50Hz.

4.1. **Design Specifications**

The design requirements were to obtain variable stator voltage, variable stator frequency below and above 50Hz a certain phase sequence.

Basing on the design specifications, the most suitable method was the Volt/Hz control because it requires very simple tuning in the form of its offset trimming and change of voltage to frequency ratio. An even stator measurement and a feedback is not required.

4.2 Drive System Schematic

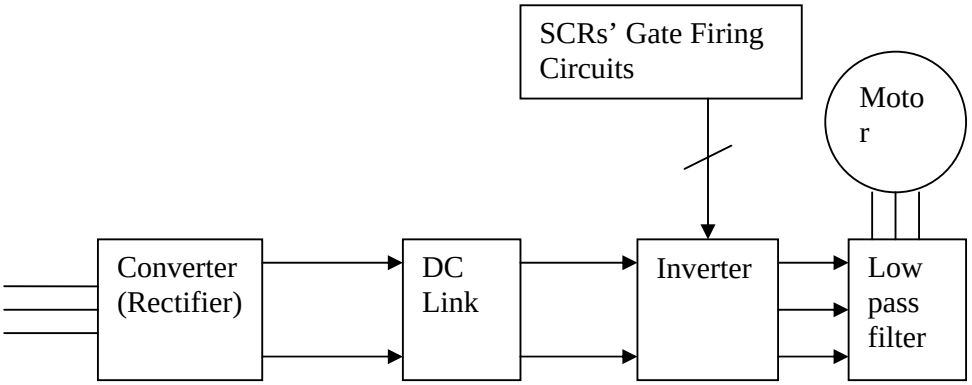


Fig.4.1 the Drive system Schematic

This is the V/Hz control drive schematic. The 555 timer connected in a monostable mode generates the PWM waveform. The change in frequency of the square waveform varies the frequency of the inverter thus varying the output voltage to the motor. The output of the multivibrator clocks the Johnson Counter whose output drove the logic circuit. The output current of TTL is in the order of microamperes hence there was need to amplify it to the required value to drive the thyristor gates. The output signal had distortions hence was filtered to eliminate harmonics before being fed to the motor.

5. THE DESIGN AND SIMULATION

The design was sub-divided into constituent sub-systems of the schematic diagram

5.1 SCRs Gate Firing Circuits

Silicon controlled rectifiers are three terminal devices .For operation to control power; the gate drive circuits must be carefully designed. The design considered the gate trigger current I_G and trigger voltage V_G for the thyristors.

5.1.1 Square Wave Generator

The square wave generator was designed by use of a 555 timer configured as a monostable multivibrator. Modulating the threshold voltage, V_{TH} varied T. Another 555 timer configured as astable multivibrator was used as a pulse generator. The generated pulses from the astable were used to drive the monostable multivibrator. The output of the monostable was at the same frequency as the pulse generator, but with pulses of variable width. This is pulse-width modulation (PWM).The output of the astable multivibrator was a constant pulse -width pulse-train with a variable repetition rate. This is pulse-position modulation (PPM).

Design of astable multivibrator

To realize a 555-timer astable, the circuit is as shown in fig.5.1

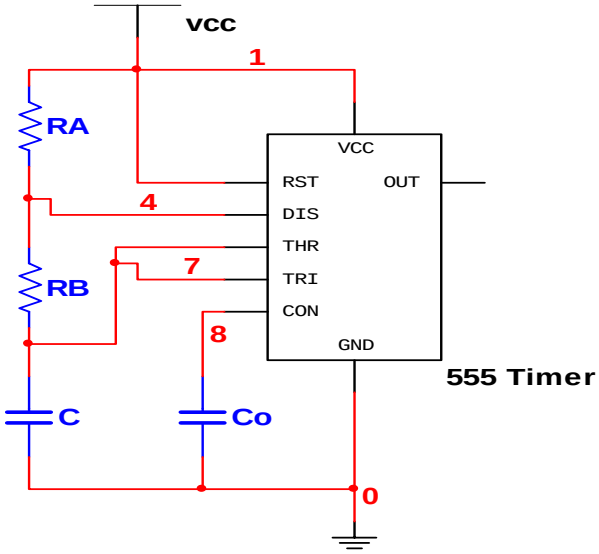


Fig.5.1 the astable multivibrator

The output waveform of the astable is usually as shown in fig.5.2

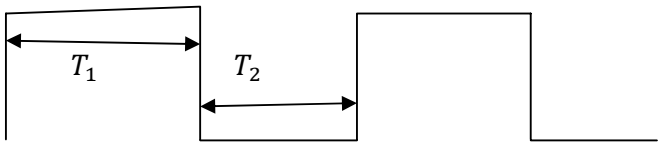


Fig.5.2 output waveform of astable

$T1$ and T2 are turn-on and turn-off times respectively.

The values of RA, RB and C were chosen to be 5k, 100k and 100nF respectively. The value of Co is always 10nF. RA, RB and C were then used to calculate the turn-on and turn-off times as follows:

$$T1 = (Ra + RB) \times \llbracket C\ ln \rrbracket\ \ 2 \quad (5.1)$$

$$= (5k + 100k) \times C \times 0.693$$

$$= (5k + 100k) \times 100nF \times 0.693$$

$$= 7.28ms$$

$$T2 = 0.693RB \times C \quad (5.2)$$

$$= 6.93ms$$

The period T of the waveform is

$$T = T1 + T2 \quad (5.3)$$

$$= (7.28 + 6.93)ms$$

$$= 14.21ms$$

The output frequency of the astable is the inverse of the period,

$$f = 1/T \quad (5.4)$$

$$= 1/14.1ms$$

$$= 70Hz$$

The duty cycle of a waveform is the ratio of the time when the output voltage is LOW to the total period;

$$D = T2/T \quad (5.5)$$

$$= 6.93ms/14.21ms$$

$$= 0.488$$

$$= 48.8\%$$

The simulation in Proteus gave the waveform in fig.5.3

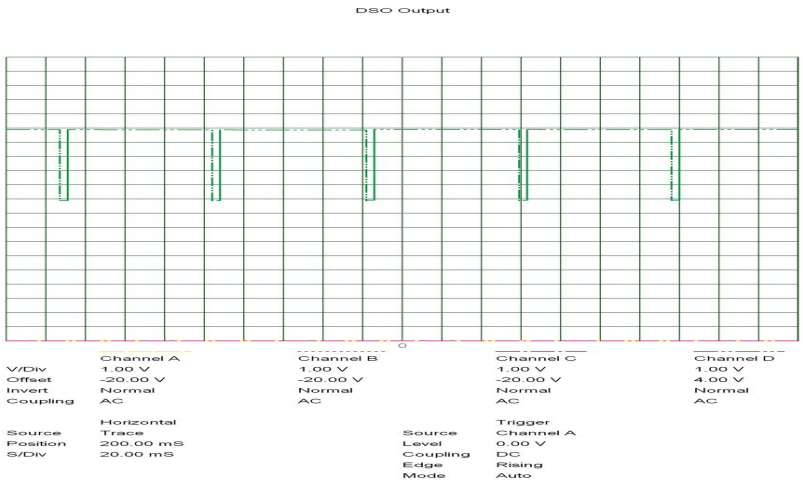


Figure 5.3 the output waveform of astable multivibrator

The output frequency of the astable was varied by varying the 10K potentiometer in series with R_A.

Design of a monostable multivibrator

The monostable Multivibrator was used as the base oscillator to generate pulses.

To realize a 555 timer monostable multivibrator, the circuit is as in fig.5.4

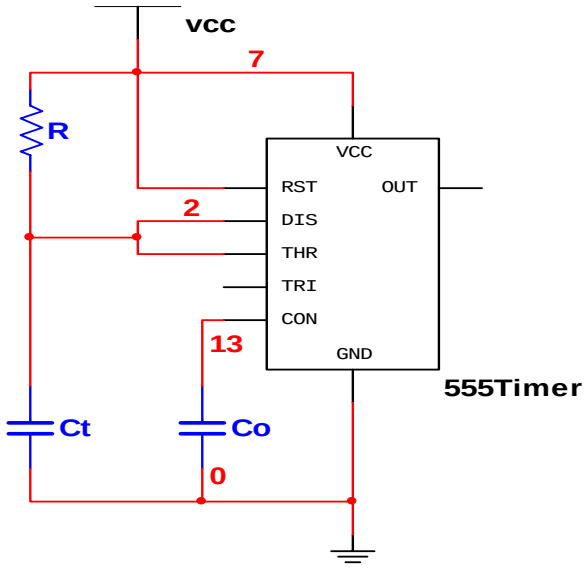


Fig.5.4 Circuit for monostable operation

The time that the output is held high is given by equation (5.6)

$$T = 1.1R \times Ct \qquad (5.6)$$

$$= 1.1 \times 3.3K \times 47nF$$

$$= 1.1 \times 3.3K \times 47nF$$

$$= 0.17ms$$

The output of the monostable was the clock the Johnson counter. Pulse width modulation in the monostable resulted in variation of the switching frequency of the counter accordingly. The output of the (base oscillator) square wave generator is as shown in fig.5.5

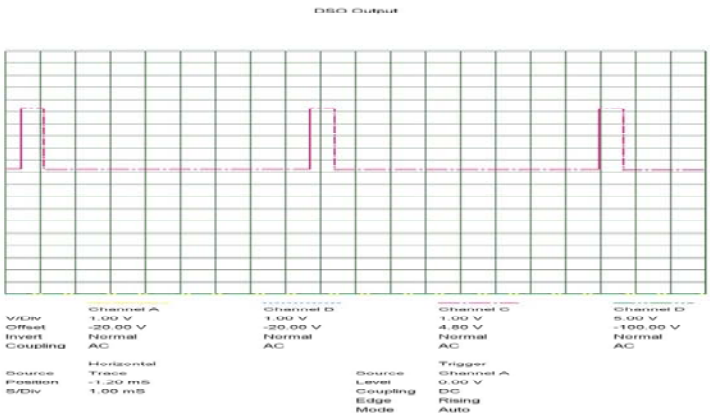


Fig. 5.5 output waveform of monostable

5.1.2 Johnson Counter and Logic Circuit

This counter gives ten outputs. After every clock pulse, only one output is HIGH while the rest are LOW. This means that logic 1 is circulated and thus the Johnson counter is a kind of a ring counter.

To switch the six SCRs forming the inverter, six signals were required. To ensure that only six outputs were from the counter, pin15 that is the master reset was connected to pin6, thus the counter was reset after every sixth count (0101)

The design required that two SCRs were ON at any instant. This was achieved by use OR gates as shown in fig. Note that there are seven outputs where as only six gating signals are required to trigger the SRCs. The switching waveforms are shown in fig. 5.6.

From fig.5.6, it was verified that before output of the first gate went off, the second gate output came on. When the second gate output had been ON for half time, the first one went off while the third came ON .The sequence continued until when the seventh gate output was ON when the first gate output came on and the cycle was repeated. The sequence continued as long the counter was running. The firing sequence of the SCRs was 12, 23, 34,

45, 56, and 61. Two SCRs were ON at any instant. This is the 120° switching sequence. In one period, that is after every 360° all the six SCRs were turned on switched.

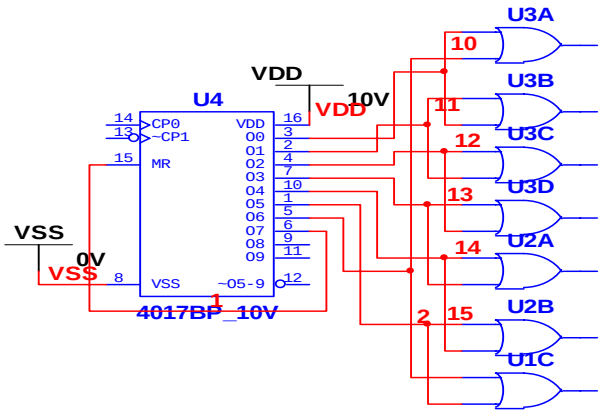


Fig.5.5 the Johnson counter and the logic circuit

60° G1

G2

G3

G4

G5

G6

Fig.5.6 gate triggering waveforms

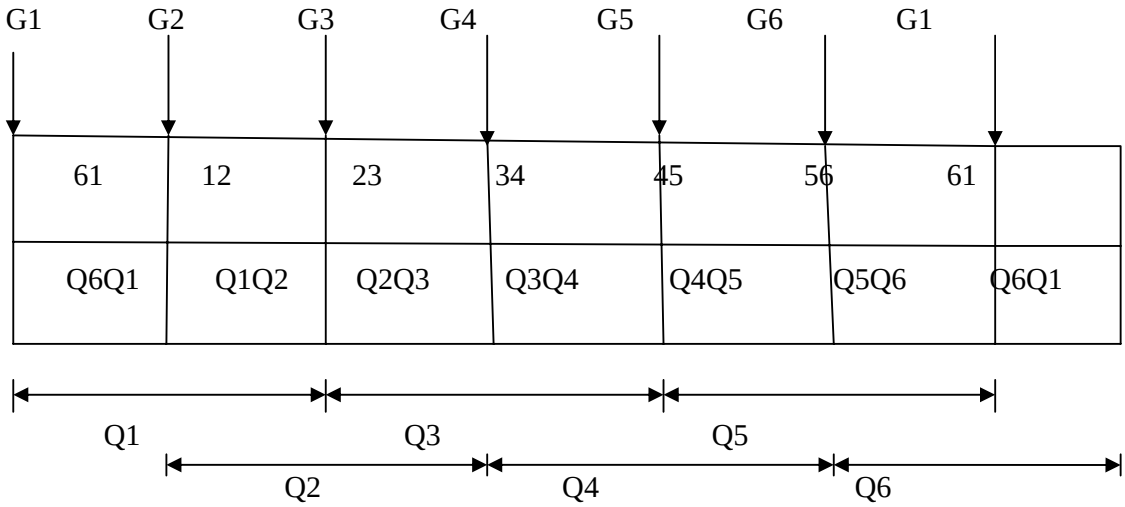


Fig.5.7 the block diagram of firing sequence of thyristors

From the block diagram, it is clear that at any given instant; two SCRs are ON for 120° each. If Q1 is considered, for example, it is turned ON whenQ6 has been on for half time. When Q1 has been ON for half time, Q2 turn ON while Q6 turns OFF. The process continued continues until all the six SCRs have been switched in one period of 360°.The naming of SCRs is considering to obtain the desired switching sequence. The simulation results for the switching sequence are shown in figure5.8

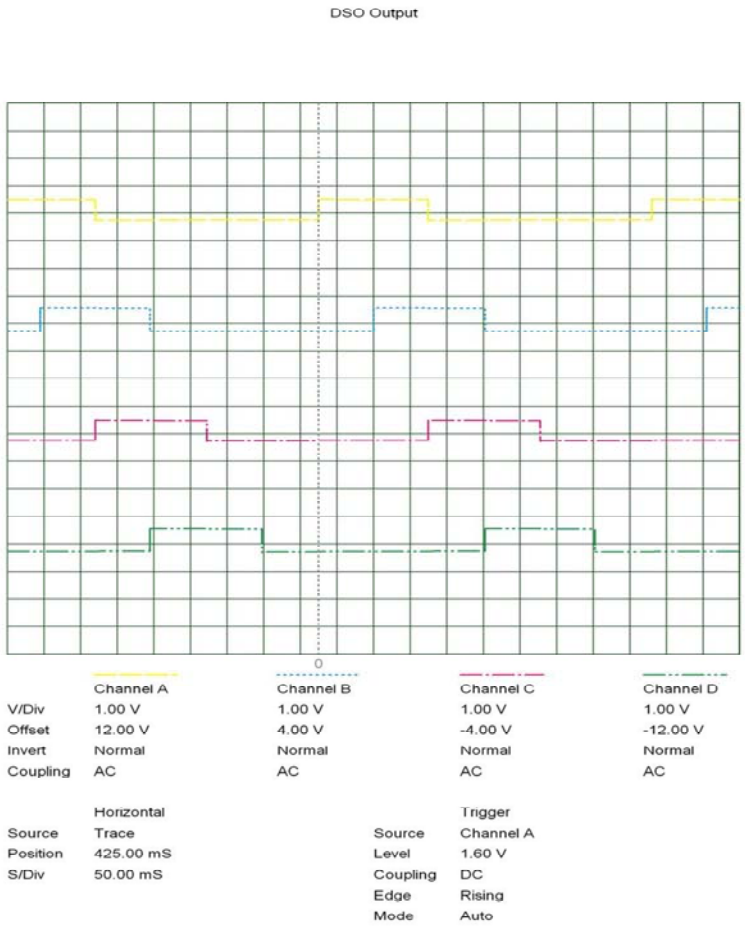


Fig 5.8 simulation waveforms for the switching sequence

5.1.3 Single Stage Transistor Amplifier

The Logic1 and logic0 output voltages for the OR gates are 5v and 0v respectively while the logic1 and logic0 input currents are 0.4mA and 8mA respectively. The SCRs that were used needed the gate trigger voltage and current of $Vgt = 1V$ and $Igt \leq$32mA respectively. This called for the use of common collector single stage transistor amplifiers to amplify the current. The 5V voltage realized by is obtained from the logic OR gates. This voltage is reduced to a lower value 1V to avoid destroying the SCR gates by dropping it across a resistor. The common collector amplifier was used since it has a high current gain, a voltage gain of less than unity and it does not invert the signal.

5.2 The PWM Inverter

This is composed of the rectifier, the constant dc link and the inverter as shown in Fig.3.1.

5.2.1 The rectifier

The uncontrolled three-phase rectifier (ordinary diodes) was designed as follows:

$$Vdc = 6/\Pi \int_0^{\pi/6} \sqrt{3}\ Vm \cos \omega t\, d\omega t \qquad (5.7)$$

$$= \frac{3\sqrt{3}}{\pi} \times Vm$$

$$= 1.654Vm$$

Where Vm is the peak phase voltage of the source

$$Vm = Vph = 110V$$

Thus $$Vdc = 1.654 \times 110 = 181.9V$$

The rms output voltage is

$$Vrms = \sqrt{[\frac{6}{\pi} \int_0^{\pi/6} 3Vm\text{^}2 \times \cos\text{^}2\omega t d\omega t\ ]} \qquad (5.8)$$

$$= \sqrt{[1.5 + \left(\frac{5.196}{4\pi}\right)]Vm}$$

$$= 1.6554Vm$$

$$= 1.6554 \times 110$$

$$= 182V$$

The load to be driven is inductive with the load current of 10.5A.This is the current Idc drawn from the rectifier. The ratings of rectifying diodes are specified in terms of average current Id, peak current Ip, rms current $Irms$ and peak inverse voltagePIV.

$$Idc = 10.5A$$

$$Id = \frac{Idc}{3} A$$

$$= 10.5/3\ A$$

$$= 3.5A$$

The rms current, $$Id\ rms = \frac{Idc}{\sqrt{3}}$$

$$= \frac{10.5}{\sqrt{3}} A$$

$$= 6A$$

The peak inverse voltage (PIV) is give by

$$PIV = \sqrt{3}Vm$$

$$PIV = \sqrt{3} \times 110$$

$$= 191\ V$$

The Fig.5.8 shows the output of the three-phase rectifier

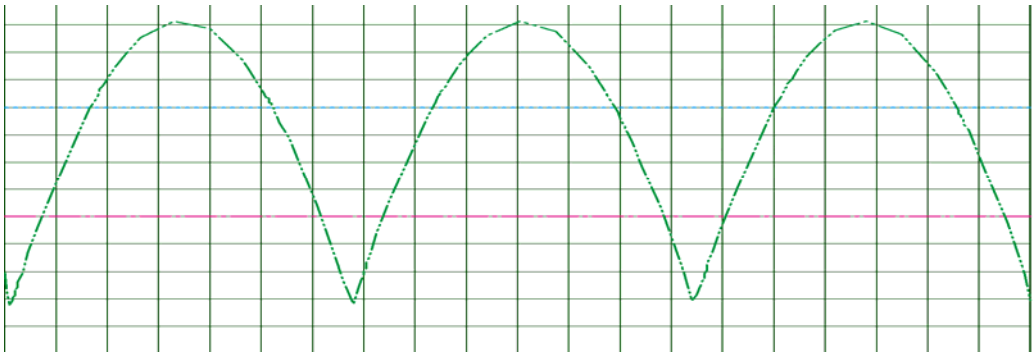


Fig.5.8 Unfiltered rectifier output

5.2.2 The DC Link

From figure, it is shown that the output of the rectifiers contain harmonics. The LC filter, which is a constant DC Link, was designed to smooth out the dc output voltage of the rectifier. The equivalent circuit for the harmonics is as shown in fig.5.9

To make it easier for the nth harmonic ripple current to pass through the filter capacitor, the load impedance must be much greater than that of the filter capacitor. That is,

$$\sqrt{[R^2 + (n\omega l)^2]} \gg \frac{1}{n\omega Ce} \qquad (5.9)$$

The rms value of the nth harmonic component appearing on the output can be found by use of the voltage divider

$$Von = \left| -\frac{\frac{l}{n\omega Ce}}{(n\omega Le) - \frac{1}{(n\omega Ce)}} \right|^2 \text{Vn} \qquad (5.11)$$

The total ripple current due to all harmonics is

$$Vac = \sqrt{(\sum_{n=2,4,6..}^{\infty} Von^2)} \qquad (5.12)$$

The desired ripple factor, that is

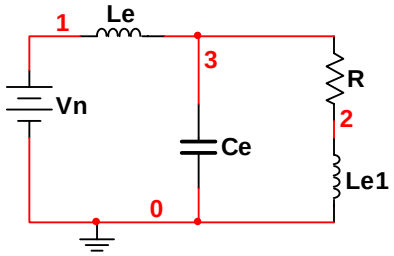
$$RF = \frac{Vac}{Vdc} = 0.1 \quad (5.13)$$

Considering the second harmonic, its rms value was obtained as

$$V2 = 4Vm/(3/\sqrt{2}\pi) \quad (5.14)$$

The dc voltage is given by

$$Vdc = 2Vm/\pi \quad (5.15)$$



Fig, 5.9 equivalent circuits for the harmonics

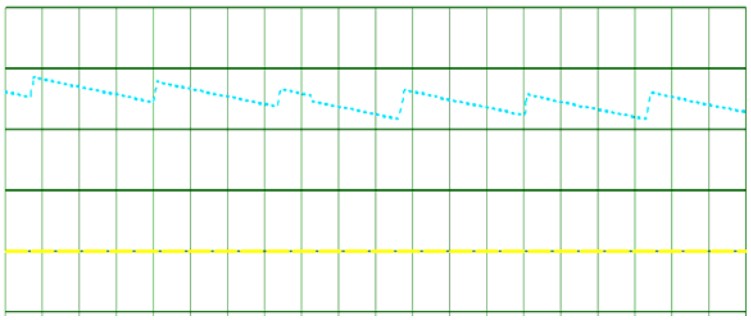


Fig.5.10 Filtered output waveform of the rectifier

6. 5.2.3 Inverter

The inverter design involved the choice of the SCRs and the method of commutation. The inverter output voltage was to vary from zero up to a maximum of 110V ac; the frequency to be varied slightly below and above 50Hz while the output current was to be 10.5A.The choice of SCRs was based on the turn on time, turn off time and the dv/dt

capability. According to the design specification, the BT 152-400R was chosen. It has the following characteristics:

$$Igt = 32mA$$

$$Vgt = 1V$$

$$Vrrm = 400V$$

$$Itsm = 200mA$$

The designed values of gate triggering current, Igt and gate triggering voltage, Vgt are 8.564mA and 856.4mV respectively.

120° Conduction Sequence

In this method, each SCR conducts for 120°.Only two SCRs remain ON at any instance of time. The gating signals for the SCRs were obtained as explained in section 5.1 and the conduction sequence is 61, 12, 23, 34, 45 and 56. The expected three -phase inverter output is as shown in fig5.11

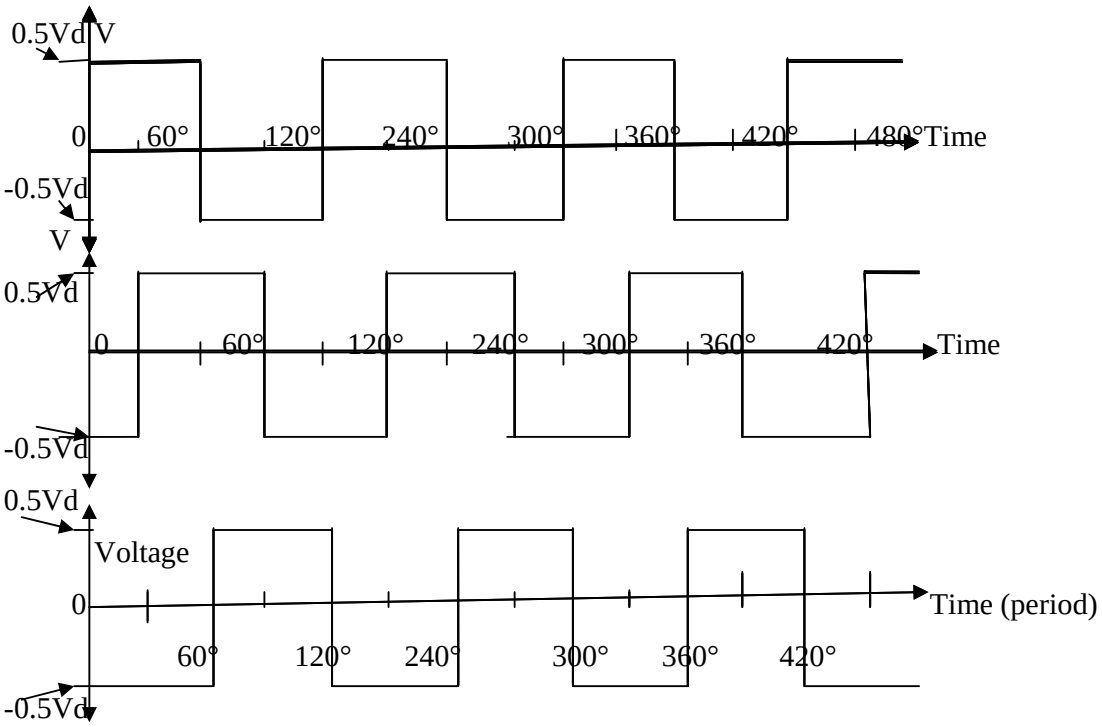


Fig.5.10 The desired output waveforms for phase voltageVa, Vb and Vc

The motor sees sinusoidal waveforms as shown in fig5.11

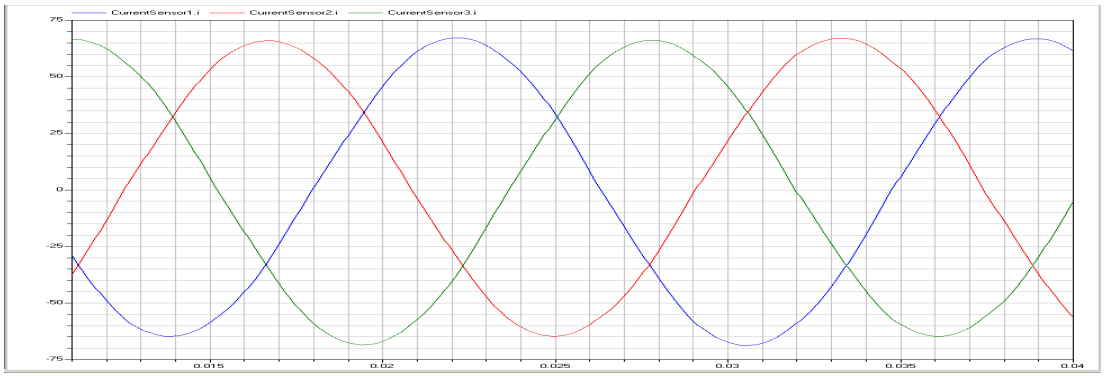


Fig.5.11 Three-phase sinusoidal waveforms

The red, green and blue lines represent the red, yellow and blue phases respectively. The blue and green waveforms lag the red waveform by 120° and 240° respectively. The simulation results for the inverter are as shown in figure24.

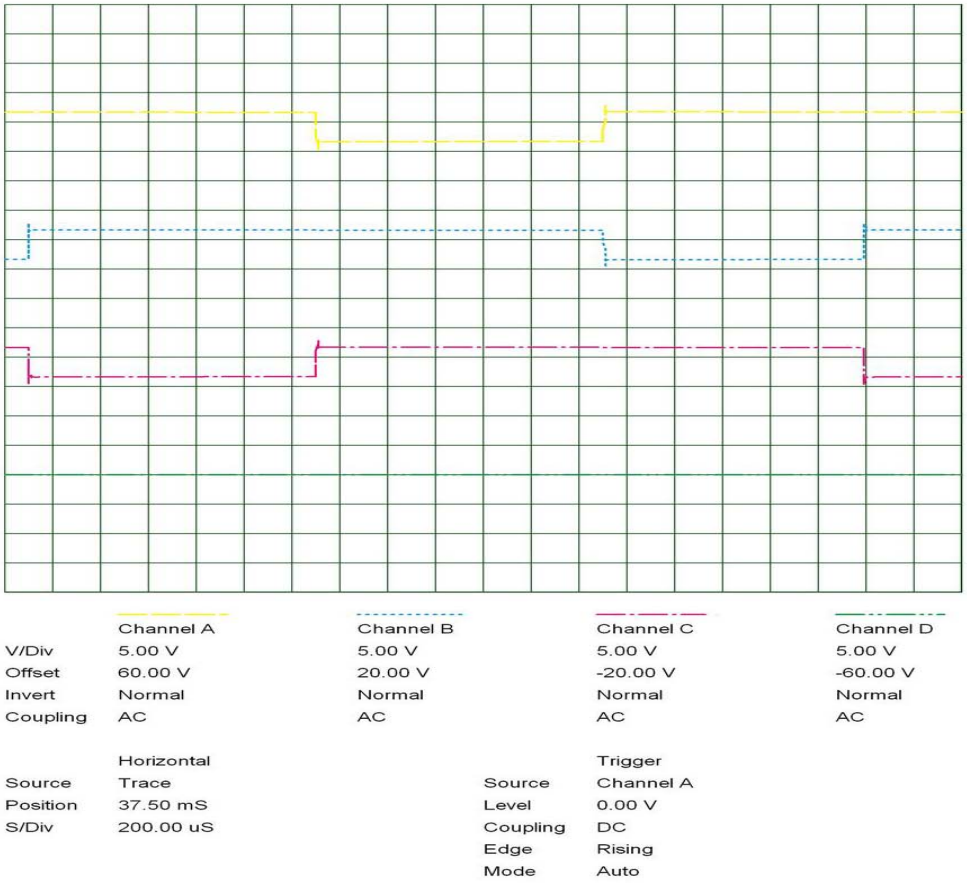


Fig .5.12 simulation waveforms for the inverter

Fourier analysis of the 3-Phase Inverter Waveforms

The application of Fourier helps in the analysis of the fundamental, the second and other higher harmonics.

a) Phase Voltage(Line-to-neutral Voltage)

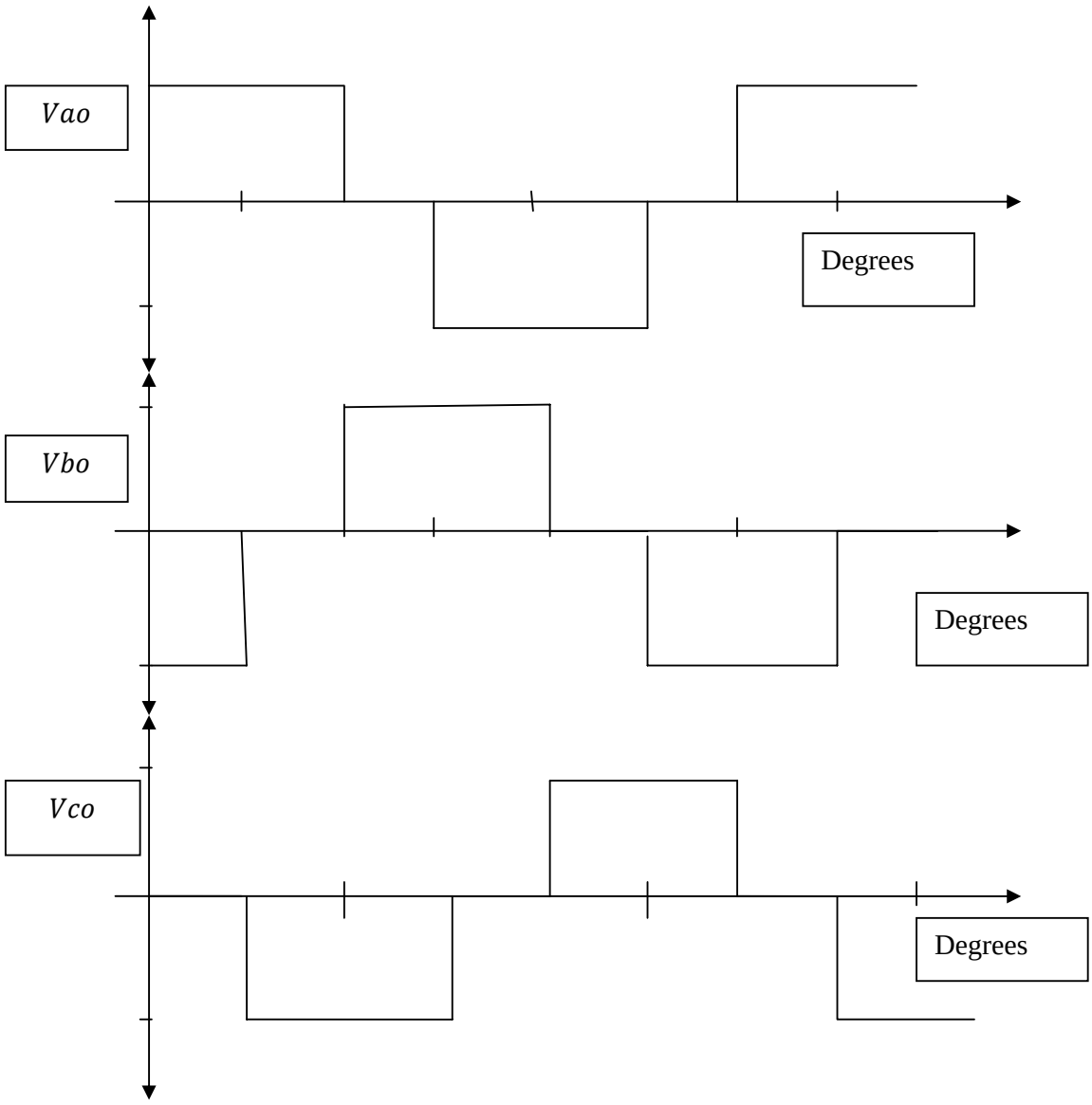


Fig.5.13 Switched dc output waveforms

The switched dc waveforms in figure 5.13 are derived from the switching sequence of the SCRs as shown in table5.1.

Table 5.1. *The Relationship between switched dc voltage and output phase voltages*

PERIOD(°)	**SCRs ON**	$\boldsymbol{Vao}$	$\boldsymbol{Vbo}$	$\boldsymbol{Vco}$
0-60	Q6Q1	$+\frac{1}{2}Vd$	$-\frac{1}{2}Vd$	0
60-120	Q1Q2	$+\frac{1}{2}Vd$	0	$-\frac{1}{2}Vd$
120-180	Q2Q3	0	$+\frac{1}{2}Vd$	$-\frac{1}{2}Vd$
180-240	Q3Q4	$-\frac{1}{2}Vd$	$+\frac{1}{2}Vd$	0
240-300	Q4Q5	$-\frac{1}{2}Vd$	0	$+\frac{1}{2}Vd$
300-360	Q5Q6	0	$-\frac{1}{2}Vd$	$+\frac{1}{2}Vd$

Applying Fourier analysis on the switched waveforms in fig.5.13, we get the following

a) Line –to –Neutral voltage waveforms(phase voltages)

$$Van = \sum_{n=1,3,5}^{\infty} \frac{2Vd}{n\pi} \cos(n\pi/6) \sin n(\omega t + \frac{\pi}{6}) \quad (5.16)$$

$$Vbn = \sum_{n=1,3,5}^{\infty} \frac{2Vd}{n\pi} \cos(n\pi/6) \sin n(\omega t - \frac{\pi}{2}) \quad (5.17)$$

$$Vcn = \sum_{n=1,3,5}^{\infty} \frac{2Vd}{n\pi} \cos(n\pi/6) \sin n(\omega t - \frac{7\pi}{6}) \quad (5.18)$$

Equations 5.16, 5.17 and 5.18 give phase voltages.

The fundamental component, when n=1, is given as

$$Va1 = \frac{2Vd}{\pi} \cos(\pi/6) \sin(\frac{\pi}{6}) \quad (5.19)$$

Vd is the dc input voltage to the inverter; the value was Vd=110V

The first harmonic of Va when n=1 was calculated as follows

$$A1 = Va1(peak) = 2Vd/\pi \quad (5.20)$$

$$A1 = 2 \times 110/\pi$$

$$= 70\text{V}$$

The rms value of the fundamental

$$Va(rms) = \frac{\sqrt{2} \times Vd}{\pi} \quad (5.21)$$

The design value of the fundamental,

$$Va(rms) = \sqrt{2} \times 110/\pi$$
$$= 49.5V$$

From the circuit simulation,

$$Va(rms) = 55V$$

This value is acceptable in the ideal there are losses thus a higher is expected.

The second harmonic when n=2 is given by

$$A2 = Va2(peak) = \sqrt{3} \times Vd/3\pi \quad (5.22)$$

$$V2(rms) = \frac{A2}{\sqrt{2}} = \sqrt{6} \times \frac{Vd}{6\pi} \quad (5.23)$$

As a ratio of the fundamental,

$$\frac{A2}{A1} = \frac{\sqrt{3} \times Vd}{3\pi} \times \frac{\pi}{2Vd}$$
$$= \frac{\sqrt{3}}{6}$$
$$= 29\%$$

This second is removed by filtering; otherwise, it will interfere with the fundamental component that is required. Just like the second harmonic, the other higher harmonics ought to be filtered out.

b) Line –to –line voltage waveforms(Vab, Vbc, Vca)

The line voltages calculated by multiplying the phase voltages by$\sqrt{3}$. These gives rise to equation 5.24, 5.25 and 5.26

$$Vab = \sqrt{3} \times Van \quad (5.24)$$

$$Vbc = \sqrt{3} \times Vbn \quad (5.25)$$

$$Vca = \sqrt{3} \times Vcn \quad (5.26)$$

The fundamental values, when n=1

$$Vab(peak) = \frac{2\sqrt{3}}{\pi} Vd \quad (5.27)$$
$$= \frac{2\sqrt{3}}{\pi} \times 110$$
$$= 121.3V$$

$$Vab(rms) = \frac{A1}{\sqrt{2}} = \frac{\sqrt{6} \times Vd}{\pi} \quad (5.28)$$
$$= \frac{\sqrt{6} \times 110}{\pi}$$
$$Vab(rms) = 85.8V$$

There is a phase advancement of 30° in the line voltages.

It is clear from table1 that at any instant, two load terminals are connected to the ac supply and the third one remains open.

5.2.3.1 Commutation

The turn off time of the thyristor varies between 5 μs and 50μs. This enables the calculation of the values of commutation inductance Lm and capacitance Cm as follows

$$t(off)max = \frac{\pi}{3} \times \sqrt{2LmCm}$$

Choosing the maximum turn off time as 30 μs, and the value of the commutating inductance Cm=100μF; the value of Lm was calculated as

$$30\times 10^{-6} = \frac{\pi}{3} \times \sqrt{2 \times 100 \times 10^{-9} \times Lm}$$

Lm = 4.1mH

The dc input voltage to the inverter $Vd = 110V$ and the required load current $Im = 10.5A$

$$\omega = \frac{1}{\sqrt{2LmCm}} = 2\pi f \qquad (5.29)$$

The maximum commutation frequency was thus calculated using equation (5.29) as follows

$$f = \frac{1}{2\pi\sqrt{2LmCm}}$$

$$= \frac{1}{2\times\pi\times\sqrt{2\times0.004\times100\times10^{-9}}}$$

$$= 5656\ Hz$$

The desired output frequency was to vary between 45Hz and 60Hz; the

$$X = \frac{Im}{Vd} \times \sqrt{\frac{2Lm}{Cm}}$$

$$= \frac{10.5}{110} \times \sqrt{\frac{2\times0.004}{100\times10^{-6}}}$$

$$= 7.6$$

The available turn of time

$$t - off = \sqrt{[2LmCm]}\ [1/\ [\cos^{-1}\frac{1}{2\sqrt{1+x^2}} - \tan^{-1}x]]$$

$$t - off = \sqrt{2} \times 0.004 \times 100 \times 10^{-6} \times [1/\cos^{-1}\frac{1}{2\sqrt{(1+(7.6)^2)}} - \tan^{-1}7.6]$$

$$= 9.4\mu s$$

This designed value of the available turn off time is within the range of operation of the practical circuit. It was hard to get a ready-made inductor of the designed value in the market. The inverter that was designed was therefore a prototype. The values of inductance and capacitance used for the commutation were hence reduced to 100nH and 100nF respectively. These gave a maximum turn off time of1.48ns. This turn off time was not enough to

completely turn off the SCRs and hence the inverter output waveforms as seen in figure5.12 are not symmetrical.

EXPERIMENTAL RESULTS

Experimental results for the firing circuit are presented in this section. The figures 6.1, 6.2 and 6.3respectively illustrate the photographs of the output waveforms of the astable multivibrator, the base oscillator (monostable) and firing signals from the amplifier stages. These experimental waveforms resemble the simulation results; however, the values of the voltage and current are greatly reduced. The sources of errors are temperature variations, losses due to connection cable resistance and power dissipations in the transistor.

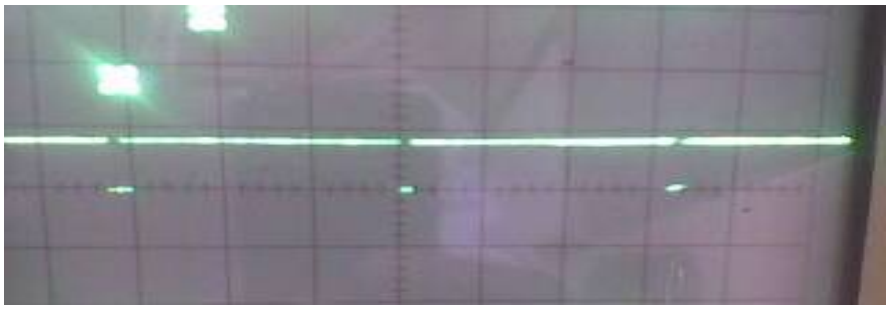


Fig.6.1 The output waveform of the astable multivibrator

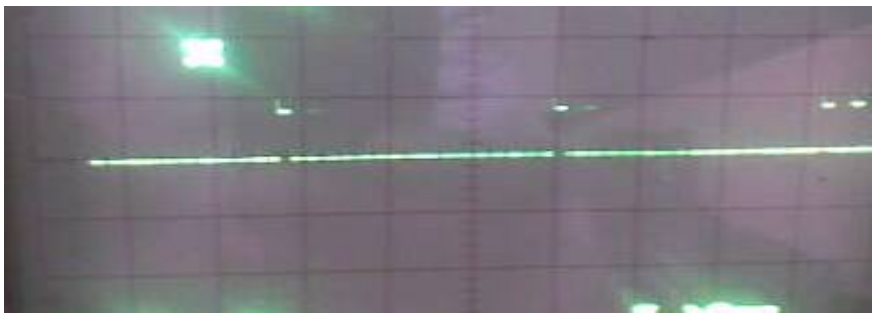


Fig. 6.2 The output waveform of the monostable multivibrator

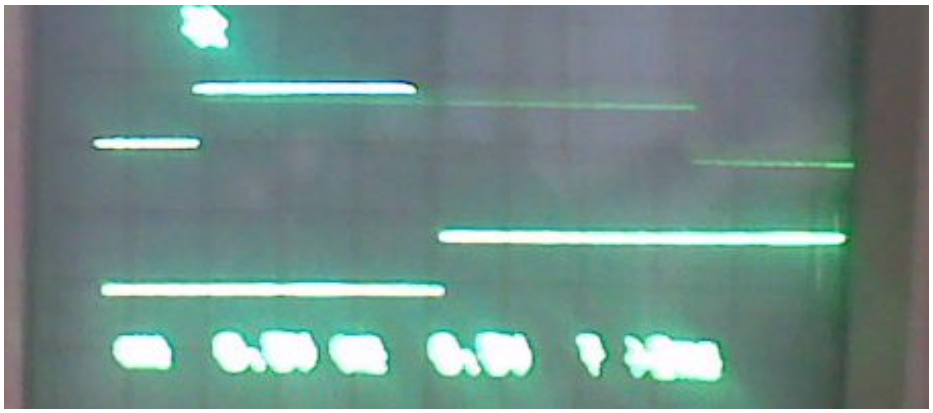


Fig.6.3 The Gate firing signals

Only two waveforms were observed at a given time since only two channel oscilloscopes were available in the laboratory.

The prototype inverter was also experimentally tested but unfortunately it did not work. This was due change in the gate properties of the SCRs during the soldering process where higher temperatures were involved.

7. CONCLUSION AND RECOMMENDATION

The theory of operation of the 3- phase synchronous motor was covered. The available motor in the laboratory then operated at 50Hz. The overall design of the inverter required the design of the ac-dc converter, the gate firing circuit, the commutation circuit and the inverter; the circuit simulations done in Proteus Professional version 7.4.The firing circuit was built on a PCB and tested in the laboratory; it was successfully done. The prototype inverter was tested in the laboratory; the gate firing for the signal for the SCRs being obtained from the built firing circuit.

7.1 Recommendations

The project required more time than the allocated time basing on the fact that all the sub-systems of the drive schematic system were designed separately. It is recommended that there be provision of a mounting board for thyristors in the electric machines laboratory with heat sinks intact to avoid soldering of SCRs as they have delicate gate that are easily destroyed by high soldering temperatures; this give results. Since the firing was successfully done, it is recommended that the next project uses this design to drive the inverter instead of redesigning the same .This will ensure more time to work on the commutation which was the biggest problem in this project.

7.2 Future Work:

There is much work to be done on the commutation circuit of the SCRs. Part of the failings of this project was the attempt to complete the work in too short a time. Much work went into the individual sub projects .The design of the firing circuits took most of the time thus design of the commutation circuit was not satisfactorily done. The next project, therefore, should entail the use of the designed firing circuit to implement the designed inverter on the available synchronous motor.

APPENDIX A

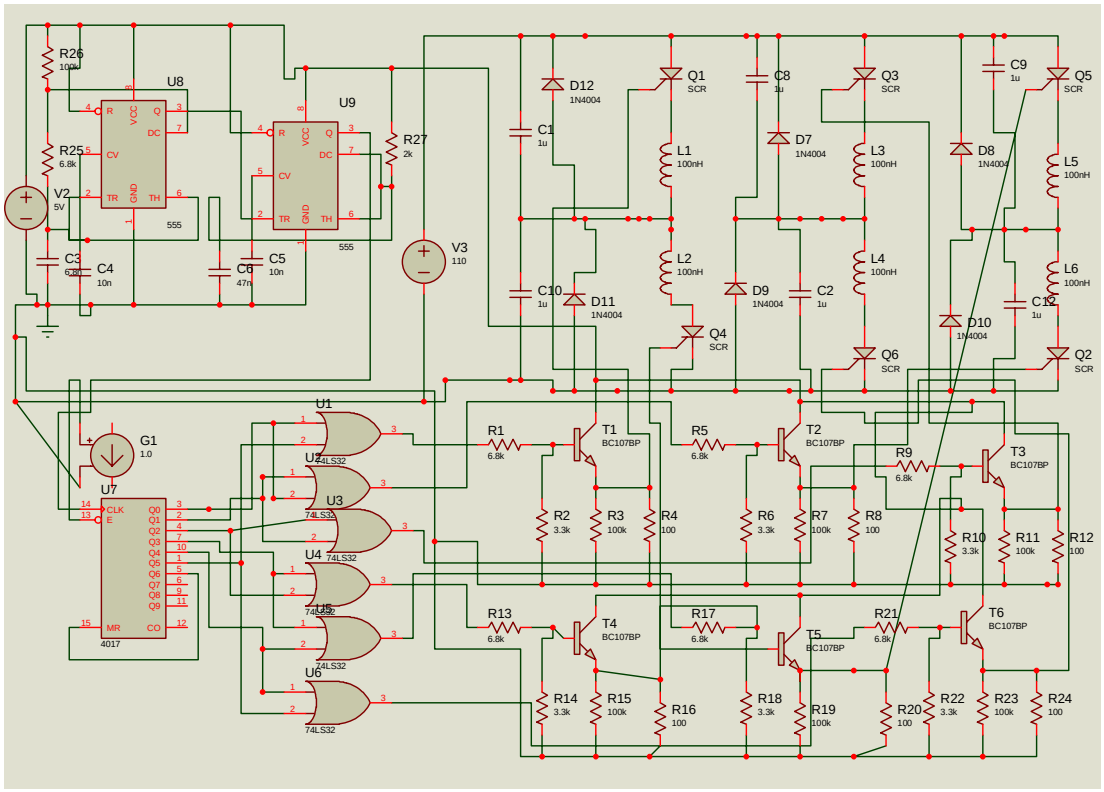


Figure A.1 The complete circuit diagram of the inverter

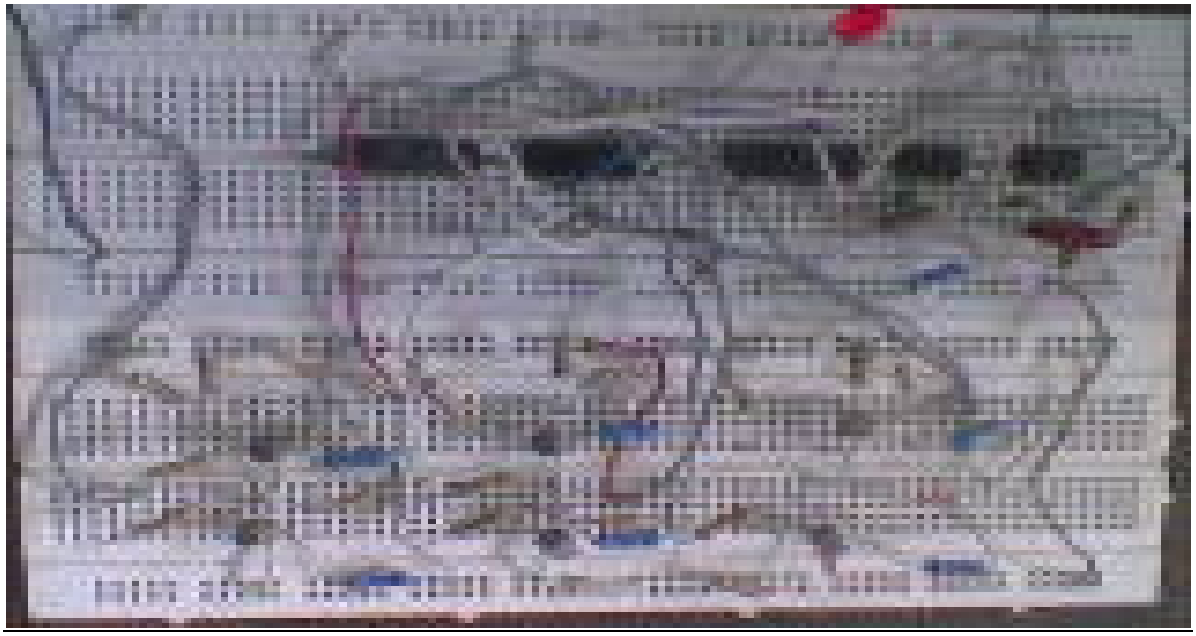


Fig.A.2 The photograph of the implemented firing circuit

APPENDIX B

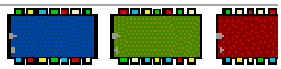
TTL

These devices make use of bipolar transistors. The main distinguishing features of the basic TTL family is that they demand a power rail which is very close to +5V, and they use a relatively high amount of current to drive their logic levels (below 1V for a logical '0' or '*low*', and above about 3.5V for a logical '1' or '*high*').

A particular characteristic of TTL signals is that the inputs to a gate "float high" — i.e. rise to a logical '1' — if left unconnected. This means that the main requirement for driving a TTL input is to "pull down" the level to near 0V. This typically takes a few milliamps per input. This is usually described by saying that a TTL signal source has to be able to "sink" a relatively large current. Typically, TTL gates take around 10-20 nanoseconds to switch level. Hence, we can 'clock' TTL and pass bits through the gates at rates up to around 50MHz provided the circuits are designed carefully. With care, speeds approaching 100MHz are possible, but for high-speed operation, other forms of logic may work better. Examples of TTL logic gates include AND gates, OR gates. NOR gates, XOR gates, NAND gates and INVERTER gates

As with other kinds of integrated circuits, there are many variations on the basic TTL family. The original chips have numbers like "SN74*xx*", where *xx* is the part number. In general, the most useful series is the SN74LS*xx* family. These consume much less current that basic TTL and hence are easier on the power supply. The 'L' in the title stands for "low power", and the 'S' stands for "Schottky" — the kinds of diode used inside the gates to help them run quickly without using a lot of current. (The diodes prevent the transistors inside the chip from 'saturating' when turned on and wasting lots of current.)

TABLE 2 *Basic Properties of some TTL Families*

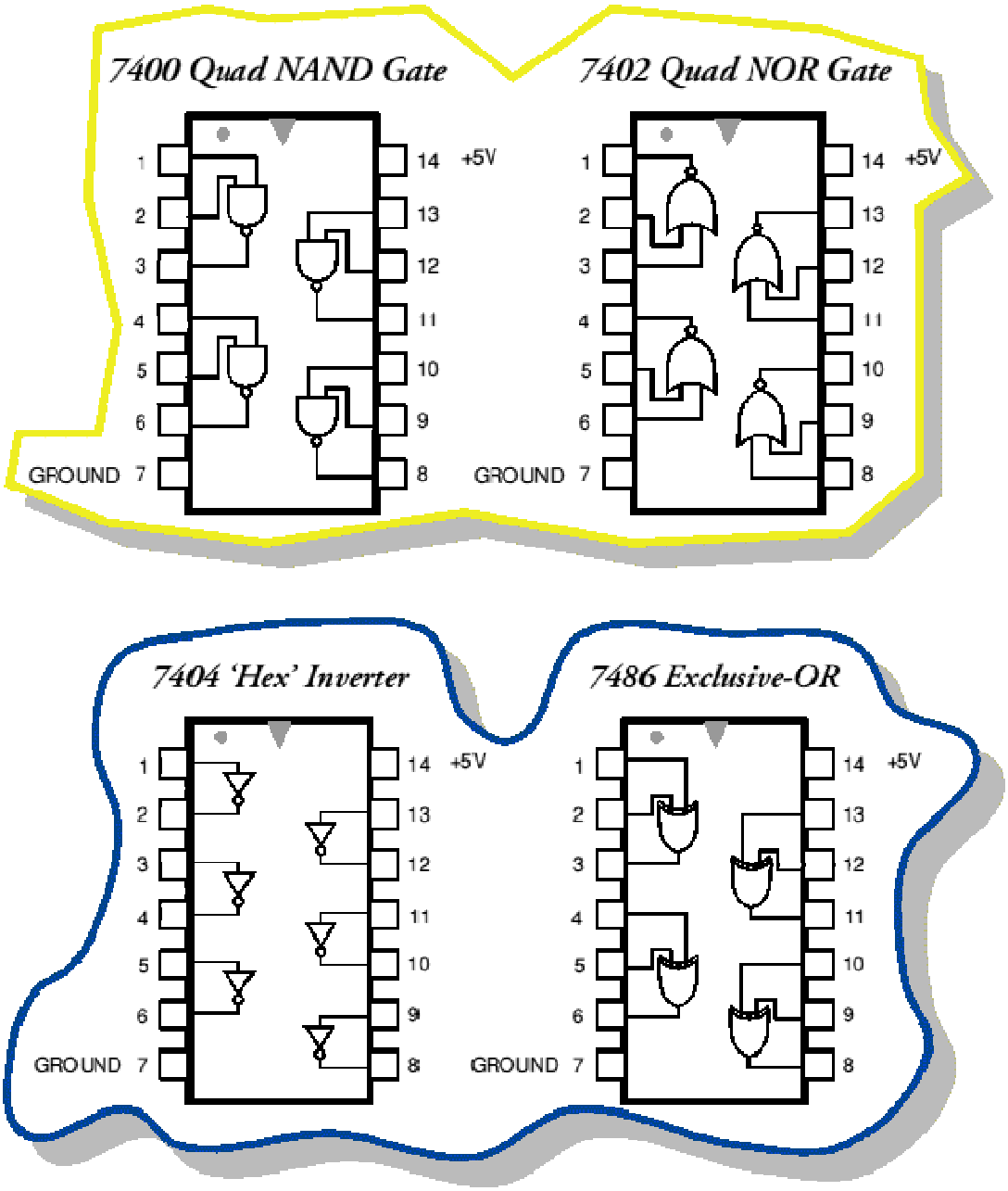
	**74 family**	**74LS family**	**54 family**
Supply Voltage	+5V (+/- 0.5V)	+5V (+/- 0.5V)	+5V (+/- 0.25V)
'1' Level Output Current	0.4mA	0.4mA	0.4mA
'0' Level Output Current	16mA	8mA	16mA
'1' Level Input Voltage (min)	2V	2V	2V
'0' Level Input Voltage (max)	0.8V	0.8V	0.8V

‘1’ Level Input Current	0.04mA	0.05mA	0.04mA
‘0’ Level Input Current	1.6mA	0.4mA	1.6mA

Comparing the above we can see that the main difference between the 74 and 74LS families is that we have to pull (i.e. ‘sink’) around 1.6mA out of a 74 input to hold it down to a logic ‘0’, but we only have to draw 0.4mA out of a 74LS to hold it down. In general, we can expect an LS gate to consume around a quarter the power/current of a plain 74 gate of the same type. Hence, the LS gates are a good choice if we are using a battery or want to save on the power supply cost.

From the table it is not obvious why anyone would choose the related 54 family as it seems much the same as the 74 one. However, 54 gates are built to operate over a much wider temperature range (-55 Celsius to +125 Celsius) that the 74/74LS (0 to 70 Celsius). Hence, the 54 family is better if we have to build circuits for ‘extreme’ environments.

TTL is still used a lot when building ‘one off’ logic circuits as the gates are cheap and robust (i.e. you are not likely to damage them when building the circuit!). However, most modern large-scale commercial and industrial systems use CMOS logic, as it is cheaper/better for integrated systems. The main disadvantage of CMOS is that it is static sensitive; hence, it can be depressingly easy to destroy CMOS logic simply by taking it out of its package carelessly.



Examples of TTL Logic Gates

APPENDIX C

Phase controlled thyristors (SCRs)

They operate at line frequency and are turned off by line commutation. Turn off time tq, is of order of 50 to 100 microseconds. These SCRs are the most suited for low speed applications and is known as converter thyristor. It's on state voltage VT is typically 1.15v for 600v and 2.5v for 4000v devices

.

Fast switching thyristors

They are used in high-speed switching applications with forced commutation e.g. in choppers and inverters. Have first turn off time generally 5 to 50 microseconds depending on the range of voltage. The on state forward drop varies approximately as a function of turn off time to. This type of thyristor is also known as inverter. Inverter thyristors with a very limited reverse blocking capability, typically 10v and very fast turn off time of between 3-5 microseconds are called asymmetrical thyristors (ASCRs).

Gate Turn off thyristors (GTO)

They turn ON by positive signals but can be turned off by a negative gate signal. They are turned ON by applying a short positive pulse and turned off by a short negative pulse to its gate.

Advantages of GTOs over SCRs are:

- elimination of commutating elements in forced commutation
- reduction in acoustic and electromagnetic noise due to elimination of commutation choke
- a high ratio of peak surge current to average current(10:1)
- high on state gain (anode /gate current) typically 600v
- is a pulsed signal of short duration

Its disadvantage is that it has higher on state voltage than SCRs

Triacs

They can conduct in both directions and are used in ac phase control. Are two SCRs connected in anti-parallel common gate connections.

Reverse conducting thyristors

In many choppers and inverter circuits, an anti- parallel diode is connected across an SCR in order to allow reverse current flow due to inductive load and to improve on turn –off requirements of the commutation circuit. The diode clamps the reverse blocking voltage of the SCR to 1 or 2 under steady state conditions. It is also called Asymmetrical thyristor.

Static inductive thyristors

They are turned on by applying a positive gate voltage and turned off by applying a negative gate voltage.

MOS –Controlled Thyristors

They use features of regenerative four-layer thyristor and MOS gate structure.

FET Controlled SCR

This combines MOSFET and thyristor in parallel. This type of SCRs is applied where optical firing is to be used for providing electrical isolation between input or control signal and switching device of power converter.

Light Activated SCR

They are turned on by direct radiation on the silicon wafer with light. Electron-hole pairs that are created due to radiation produce triggering current under influence of electric field. The gate structure is designed to provide sufficient gate sensitivity for triggering from practical light sources. They are used in high –voltage and high-current applications

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