DATA-AIDED CARRIER RECOVERY WITH QUADRATURE PHASE SHIFT-KEYING MODULATION

BY
AUDI VALENTINE OTIENO
REGISTRATION NUMBER: F17/38919/2011

SUPERVISOR: PROF. V. K. ODUOL

REPORT SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING IN PARTIAL FULFILMENT OF THE DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING AT THE UNIVERSITY OF NAIROBI.
DECLARATION OF ORIGINALITY

NAME OF STUDENT: AUDI VALENTINE OTIENO

REGISTRATION NUMBER: F17/38919/2011

COLLEGE: Architecture and Engineering

SCHOOL: Engineering

DEPARTMENT: Electrical and Information Engineering

COURSE: Bachelor of Science Electrical & Electronic Engineering

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DEDICATION
This work is dedicated to my parent, Mrs. Pamela Audi, who has been a motivator to excellence through diligent work and integrity.
ACKNOWLEDGEMENTS

I would like to acknowledge and especially give thanks to those who through their input and continued support have made this work a success.

First among these is the Creator, One who is the spring of all good things and through whom all things come.

Secondly, I would like to acknowledge and thank my supervisor, Professor Vitalice K. Odoul, without whose direction and guidance these work would not have been accomplished in the given time and whose input has proved to have been invaluable in its undertaking.

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Lastly, I would like to acknowledge and thanks all those who have heretofore endeavoured to carry out in this field. Much of the work in print and published have been of great help in the carrying out of the project.
EXECUTIVE SUMMARY

This work mainly discusses carrier recovery with a special focus in digital communication systems wherein Binary Phase Shift Keying and Quadrature Phase Shift Keying modulation technique is used in data modulation and demodulation. Furthermore, it highlights two main methods of carrier recovery used in this modem: the method of re-modulation, also known data-aided carrier recovery, and the Costas based carrier recovery method. The data-aided carrier recovery system was designed and demonstrated with relevant final analysis of the performance of the system. Conclusions are finally drawn giving the merits and demerits of the system and recommendations are given.
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<th>Description</th>
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<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>DCS</td>
<td>Digital Communication System</td>
</tr>
<tr>
<td>LSI</td>
<td>Large Scale Integration</td>
</tr>
<tr>
<td>ASK</td>
<td>Amplitude Shift Keying</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency Shift Keying</td>
</tr>
<tr>
<td>PSK</td>
<td>Phase Shift Keying</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-Symbol Interference</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Lock Loop</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
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CHAPTER 1: INTRODUCTION

1.1: INTRODUCTION TO THE PROJECT REPORT

In modern communication systems transfer of information through long distance is done using signals of frequencies in the microwave range. These signals travel at considerably good speed through any medium because of their high frequencies. The desired communication, message, is usually superimposed on these signals and sent through a medium then through appropriated signal processing extracted from these high frequency signals. The main method of the message extraction involves a multiplication of the modulated carrier with a signal of replica frequency and phase at the receiver end. A shift in frequency of either signal produces oscillation and the renders the message difficult to be accurately extracted. A not well synchronized system result in misinformation which is fatal.

Likewise, in the present day, communication is not only done through stationary systems. Some communication systems are usually in motion, such as a mobile handset and thus due to Doppler shift these may cause the frequency and phase of the modulated signal to slight differ from that generated by handset internally, which may have been initially at the frequency of the transmitted modulated signal. Again misinformation may result. Therefore, a system is required that is able to track the frequency of the carrier signal and ‘lock’ on it to ensure coherent demodulation. This process is termed carrier recovery.

1.2: AIMS OF THE PROJECT

The objectives of the project were:

1.) To study Phase shift keying modulation and demodulation in both Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying. (QPSK)
2.) To study synchronization through the carrier recovery with emphasis on the Costas loop method of carrier recovery and the data-aided method of carrier recovery and compare the two methods.
3.) To design and demonstrate carrier recovery through the data-aided method of carrier recovery

1.3: SCOPE OF THE PROJECT

The project handles three main areas in communication, namely;

1.) Modulation theory
2.) Demodulation theory
3.) Synchronization theory.

Modulation and demodulation theory are handles in the light of phase shift keying technique only whereas synchronization is only dealt with in the view of carrier recovery with special emphasis on re-modulation method.
CHAPTER 2: LITERATURE REVIEW

2.1: GENERAL INTRODUCTION

Digital communication systems (DCS) increasing became attractive over time compared to analog communication systems for a number of reasons. The principal reason given to be that in DCS over a given time there is only a given finite set of waveforms are transmitted whereas for an analogue system for the given time there is an infinite set of waveform that can be transmitted. (Fourier Transform) This theoretically translates to infinite resolution on the part of analogue communication systems which is impractical. Moreover, by use of regenerative repeaters, the transmitted digital signal, which can be basically viewed as a pulse, and which undergoes attenuation, distortion and noise interference in the channel of transmission can be regenerated at certain intervals. This helps achieve high signal fidelity used together with error correcting methods. [1]

Thus it can be seen that the objective of the DCS is not reproduce the transmitted signal but that from the noise affected signal reaching the receiver determine most accurately the transmitted signal. Thus an important feature of a DCS is its measure of probability error.

Beyond these some other advantages include the cost of digital processing circuits and their reliability compared to analogue circuits. Digital hardware (e.g. microprocessors and LSI) also lends itself to fabrication hence implementation as compared to analogue circuits. However, the disadvantage of digital communication system that is when the signal-to-noise ratio goes below a certain threshold the signal fidelity drastically drops.
A Digital Communication System can be well explained by the flow diagram below. [1]

Figure 2: A Digital Communication system

Simply, the diagram can be viewed as having two sections, the upper blocks and the lower blocks. In the upper section of the diagram, the format block converts the information from source into bits (i.e. through sampling, quantisation and coding) and the generated binary digits are grouped into digital messages or symbols. From that point to the pulse modulation block the signal is in the form of bit stream. ... For Radio frequency transmission the digital baseband waveform is frequency translated to the carrier frequency under bandpass modulation and finally transmitted through the antenna.

In the lower section of the diagram the transmitted radio frequency signal is received and the inversion of the process that took place in the Upper section achieved. Among these are demodulation which are seen under the blocks “demodulate & sample” and “detect blocks”. The modulate, demodulate/detection blocks are collectively referred to as a modem. It is on these, the modem, that our study is based on with emphasis on the later blocks.

2.2: THE MODEM

2.2.1: MODULATION

Modulation is defined as the process by which message symbols or channel symbols are converted to waveforms that are compatible with the requirements imposed by the transmission channel. Cite. This is usually achieved by use of a mixer where a baseband signal
is made to modify the characteristics of a carrier signal. Thus effectively the baseband signal is translated to the frequency of the carrier signal and its information carried in the characteristics of the signal. Generally, most carrier signals used are sinusoidal of frequency in the range of MHZ to GHZ.

The main reasons for modulation are to achieve antenna practicability and frequency division multiplexing. [1]

Given when modulating the baseband signal modifies the characteristics of the carrier wave, and it is in these characteristics that the information is stored, it follows that there are three kinds of modulation namely: Amplitude, Frequency and Phase. Even as the carrier wave is described by the equation:

\[ s(t) = A \cos (\omega_o t + \phi(t)) \]

where: 
- \( A \) is the amplitude 
- \( \omega_o \) the frequency component 
- \( \phi(t) \) the phase

### 2.2.1.1: DIGITAL MODULATION
Thus under digital modulation, we have three modulation techniques;

1.) Amplitude Shift Keying  
2.) Frequency Shift Keying  
3.) Phase Shift Keying

### 2.2.1.1.1: AMPLITUDE SHIFT KEYING
Amplitude-Shift-Keying: that utilises the amplitude characteristics of the carrier wave to store the baseband signal characteristics. [1]
2.2.1.2: FREQUENCY SHIFT KEYING

Frequency-Shift-Keying; That which utilises/modifies the frequency of the carrier wave to store baseband signal characteristics.

![Figure 4: A Diagram Illustrating (FSK) Frequency Shift Keying](image)

2.2.1.3: PHASE SHIFT KEYING

Phase-Shift-Keying; that which makes use of the phase characteristics of the carrier wave to store baseband signal characteristics.

![Figure 5: A Diagram illustrating (PSK) Phase shift Keying](image)

2.2.1.2: PHASE SHIFT KEYING

In phase modulation a constant frequency is maintained; only change the phase of the carrier signal changes. The phase of the carrier may be made to change between two waveforms of opposing phase, 180 degrees apart, when transmitting 1-bit digital signal (binary phase shift keying, BPSK) or the phase can be changed four times, 90 degrees apart when transmitting 2-bit digital signal (Quadrature phase shift keying, QPSK). The latter effectively increases the bandwidth of the carrier.

The general carrier equation and phase shift keying equation are respectively given as

\[ s(t) = A \cos (\omega t + \varphi(t)), \text{ where} \]

\[ s_i(t) = \frac{2E}{\sqrt{T}} \cos (\omega t + \varphi_i(t)), \quad \text{for} \; 0 < t < T \]
$i = 1, ..., M$

where,

A is amplitude.

E is the energy

$T$ is the signal duration

$\phi_i(t)$ is the phase of the signal

To effect the various types of phase shift keying, binary or quadrature, the phase term is usually expressed as

$$\phi_i(t) = \frac{2\pi i}{M}, \text{ where } i = 1, ..., M \quad (3)$$

Phase and frequency modulation are usually offer more immunity to noise hence are preferred over amplitude modulation.

2.2.1.2.1: BINARY PHASE SHIFT KEYING

Modulation input majorly used is a sine wave. The digital signal used to modulate it is binary and hence changes its phase between $0^\circ$ and $180^\circ$ with a change between the two logic levels. A sine wave that is $180^\circ$ out of phase with another can both be represented as antipodal signals as shown below taking the reference phase shift to be $0^\circ$. [4]

$$s_1(t) = \sqrt{\frac{2E}{T}} \cos \omega_0 t, \ 0 < t < T \text{ for digital signal 1} \quad (4)$$

$$s_2(t) = -\sqrt{\frac{2E}{T}} \cos \omega_0 t, \ 0 < t < T \text{ for digital signal 0} \quad (5)$$

The graphical representation of the BPSK signal on a signal constellation is shown below [4]

![Figure 6: A signal constellation of a BPSK signal](image-url)
These signals can also be represented on orthonormal basis functions as follows:

\[ \phi_1(t) = \sqrt{\frac{2}{T}} \cos \omega_o t \quad 0 < t < T \] ... (6)

\[ \phi_2(t) = -\sqrt{\frac{2}{T}} \sin \omega_o t \quad 0 < t < T \] ... (7)

### 2.2.1.2.1.1: BIT ERROR PROBABILITY

The bit error probability as derived from the general binary signal is defined as [4]

\[ P_b = Q \left( \sqrt{\frac{E_1 + E_2 - 2P_{12}\sqrt{E_1 E_2}}{2N_o}} \right) \] ... (8)

For BPSK, the bit error probability becomes

\[ P_b = Q \left( \frac{2E_b}{N_o} \right) \text{, since } P_{12} = -1, E_1 = E_2 = E_b \] ... (9)

### 2.2.1.2.1.2: POWER SPECTRAL DENSITY

Given the basic pulse of BPSK signal is as follows [4]

\[ P(t) = \begin{cases} A & \text{for } 0 < t < T \\ 0, & \text{otherwise} \end{cases} \] ... (10)

Its Fourier transform is

\[ G(f) = AT \frac{\sin \pi f T}{\pi f T} e^{-j2\pi f T/2} \] ... (11)

And thus the power spectral density is given as

\[ \Psi_s(f) = \frac{|G(f)|^2}{T} = A^2 T \left( \frac{\sin \pi f T}{\pi f T} \right)^2 \] ... (12)

### 2.2.1.2.1.3: BPSK MODULATOR

A BPSK modulator is simply achieved by mixing the digital signal and the carrier

![Diagam](image.png)

**Figure 7:** A diagrammatic representation of a BPSK modulator

Through multiplication of the carrier sinusoidal wave with the given bit stream the resulting waveform is a BPSK signal which has the following representation. [3]
2.2.1.2: **QPSK MODULATION**

In quadrature phase shift keying, 2-bits are represented by a symbol whereas in Binary phase shift keying, 1 bit represented a symbol. Evidently this has the advantage of increased bandwidth efficiency as now more information is transmitted in a single symbol. In the general M-ary PSK modulation technique, the relation

\[ n = \log_2 M \]  

... (13)

where,

- \( n \) represents the number of bits
- \( M \) represents the total number of set integers

In QPSK, which is generally a form of M-ary PSK, \( n = 2 \) and \( M=4 \) and the general phase keying relation holds

\[ s_i(t) = \sqrt{2E} \cos \left( \omega t + \varphi_i(t) \right), \quad \text{for } 0 < t < T \]  

... (2)

\( i = 1, ..., M \)

with \( \varphi_i(t) = \frac{2\pi i}{M} \), where \( i = 1, ..., M \)

And thus the initial phase for the four cases of \( M = 1,2,3,4 \), are \( 45^\circ, 135^\circ, 225^\circ \) and \( 315^\circ \).

Taking the original PSK modulation equation

\[ s(t) = A \cos \left[ \omega t + \phi(t) \right] \]  

... (1)

And applying geometry, it can be also be written as

\[ s(t) = A \cos \phi(t) \cos \omega t - \sin \omega t \sin \phi(t) \]  

... (14)

\[ = s_{i1} \varphi_1(t) + s_{i2} \varphi_2(t) \]  

... (15)

Where

\[ s_{i1} = \int_0^T s_{i1} \varphi(t) \, dt = \sqrt{E} \cos \varphi(t) \]  

... (16)
\[ s_{12} = \int_0^T s_{12}(t) \, dt = \sqrt{E} \sin \varphi(t) \quad \text{... (17)} \]

Given

\[ E = 0.5 A^2 T \text{ and is the symbol energy} \]

The phase is related to both \( s_{11} \) and \( s_{12} \) as follows

\[ \varphi(t) = \tan^{-1} \frac{s_{12}}{s_{11}} \quad \text{... (18)} \]

Thus for the di-bit the table below is true. [4]

<table>
<thead>
<tr>
<th>DIBIT</th>
<th>PHASE, ( \varphi )</th>
<th>( s_{11} = \sqrt{E} \cos \varphi )</th>
<th>( s_{12} = \sqrt{E} \sin \varphi )</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>( \pi/4 )</td>
<td>( \sqrt{E}/2 )</td>
<td>( \sqrt{E}/2 )</td>
</tr>
<tr>
<td>01</td>
<td>( 3\pi/4 )</td>
<td>( -\sqrt{E}/2 )</td>
<td>( \sqrt{E}/2 )</td>
</tr>
<tr>
<td>00</td>
<td>( -3\pi/4 )</td>
<td>( -\sqrt{E}/2 )</td>
<td>( -\sqrt{E}/2 )</td>
</tr>
<tr>
<td>10</td>
<td>( \pi/4 )</td>
<td>( \sqrt{E}/2 )</td>
<td>( -\sqrt{E}/2 )</td>
</tr>
</tbody>
</table>

Table 1: QPSK Phase representation

The signal constellation of a QPSK signal is shown below [4]

![QPSK constellation diagram](image)

Figure 9: QPSK representation on the constellation diagram

QPSK signal can be characterised by two orthogonal BPSK channels where the bit stream is divided into an even, \( s_{12} \) and an odd stream, \( s_{11} \). Each stream modulates an orthogonal component of the carrier at half the bit rate of the original bit stream. The even stream, denoted by I, modulates the \( \cos \omega t \) term whereas the odd stream, denoted by Q, modulates
the sin $\omega t$ term and each component vector have a value of $E/\sqrt{2}$ taken the original QPSK vector had a magnitude of $E$. Therefore, each BPSK quadrature signal has half of the average power and bit rate of the QPSK signal.

$$s(t) = A\sqrt{2} I(t) \cos \omega_c t - A\sqrt{2} Q(t) \sin \omega_c t \quad \text{for } -\infty < t < \infty \quad \ldots (19)$$

For this reason, the signal to noise ratio of the composite QPSK signal is the same as that for the BPSK signal.

$$\frac{E_b}{N_0} = \frac{s/2}{N_0} \left( \frac{W}{R/2} \right) = \frac{s}{N_0} \left( \frac{W}{R} \right) \quad \ldots (20)$$

Where  
- $E_b$ is bit energy
- $N_0$ is noise power spectral density
- $s$ is signal power
- $W$ is bandwidth
- $R$ is bit rate

2.2.1.2.2.1: BIT ERROR RATE
The bit error rate probability for QPSK, in consideration of the two orthogonal channel, is the same as that of BPSK and given as 

$$P_b = Q \left( \sqrt{\frac{E}{N_0}} \right) = Q \left( \sqrt{\frac{2E_b}{N_0}} \right), \quad \text{for coherent PSK} \quad \ldots (21)$$

2.2.1.2.2.2: POWER SPECTRAL DENSITY
The power spectral density of QPSK us similar to that of BPSK but only now narrower. It is given by 

$$\Psi_s(f) = \frac{|G(f)|^2}{T} = 2A^2 T \left( \frac{\sin \pi f T}{\pi f T} \right)^2 \quad \ldots (22)$$
2.2.1.2.2.3: QPSK MODULATOR

The diagram below is a conceptual illustration of a QPSK modulator circuit. [6]

![Diagram of QPSK Modulator](image)

Figure 10: A diagrammatic representation of a QPSK modulator

The I stream can be seen as the signal path above while the Q stream can be seen to be the signal path below. The modulation done is similar to that of the BPSK signal only now in two parallel streams. Hence the resulting waveform is that of a BPSK signal.

2.2.2: DEMODULATION

2.2.2.1: BASIC DEMODULATION CONCEPTS

Once the signal is transmitted through the channel it will have to be received at the end and the information obtained from the signal for communication to take place. The signal processing that was done on the signal will have to be reversed and the original signal obtained. This reverse process is referred to as demodulation.

The demodulation process involves a series of steps. These are mainly mixing, filtering and detection. Mixing is the multiplication of the incoming signal with the locally generated signal to yield the signal term as will be hereafter shown mathematically. Filtering is the process of removal of the high frequency component in the resultant multiplied signal and detection is the process of determination which signal was transmitted. These process can be achieved through a matched filter or a threshold detector. By this means the message signal is usually recovered.
2.2.2.2: BPSK DEMODULATOR

Below is a BPSK demodulator circuit. The carrier wave regenerate circuit is separate and through tracking it provides the necessary phase and frequency of the locally generated carrier wave for the demodulation process. [7]

![BPSK demodulator circuit diagram](image1)

Figure 11: A BPSK demodulator circuit diagram

2.2.2.3: QPSK DEMODULATOR

Likewise, below is the QPSK demodulator circuit. [7]

![QPSK demodulator circuit diagram](image2)

Figure 12: A QPSK demodulator circuit

2.2.2.4: SOME BASIC DEMODULATOR MATHEMATICAL ANALYSIS

[8] Suppose we have a local oscillator at the receiver end and considering only the sinusoidal part of the received signal without the noise term.

By Euler’s relations we know;

\[
\sin \omega t = \frac{e^{j\omega t} - e^{-j\omega t}}{j2} \quad \text{... (23)}
\]

\[
\cos \omega t = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \quad \text{... (24)}
\]

THE SINE CARRIER
At the receiver end the local oscillator is designed to produce an identical sine wave as the one used in the transmitter end for modulation. The incoming signal is hence multiplied by this generated sine wave. Assuming they are identical it follows as shown below;

\[
\sin \omega t \ast \sin \omega t = \frac{e^{j\omega t} - e^{-j\omega t}}{j2} \ast \frac{e^{j\omega t} - e^{-j\omega t}}{j2} \quad \cdots (25)
\]

\[
= \frac{e^{-j\omega t} - 2e^{0} + e^{-j\omega t}}{-4} \quad \cdots (26)
\]

given \(e^{0} = 1\)

\[
\sin \omega t \ast \sin \omega t = \frac{-2}{-4} + \frac{e^{j2\omega t} - e^{-j2\omega t}}{-4}
\]

\[
= \frac{1}{2} - \frac{1}{2} \left[ \frac{e^{j2\omega t} + e^{-j2\omega t}}{2} \right] \quad \cdots (27)
\]

By definition;

\[
\frac{e^{j2\omega t} - e^{-j2\omega t}}{2} = \cos 2\omega t
\]

Hence,

\[
\sin \omega t \ast \sin \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\omega t \quad \cdots (28)
\]

Thus it can be seen that through the demodulation process we obtain a signal with no frequency component, \(\frac{1}{2}\), which is essentially a D.C. signal, and a signal with twice the frequency of the carrier signal, but half the amplitude, \(\frac{1}{2} \cos 2\omega t\). The latter signal, in graphical representation, is usually superimposed on the former signal producing a D.C. offset effect.

**THE COSINE CARRIER**

Similarly, taking the carrier signal to be a cosine wave, multiplying it with the local oscillator signal yields,

\[
\cos \omega t \ast \sin \omega t = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \ast \frac{e^{j\omega t} - e^{-j\omega t}}{j2} \quad \cdots (29)
\]

\[
= \frac{e^{-j2\omega t} - e^{-j2\omega t}}{-j4} = \frac{1}{2} \left[ \frac{e^{j2\omega t} - e^{-j2\omega t}}{j2} \right] \quad \cdots (30)
\]

\[
= \frac{1}{2} \sin 2\omega t \quad \cdots (31)
\]

Herein, there is no D.C. offset.
This corresponds to when no information in the phase is transmitted.

**A PHASE SHIFTED CARRIER SINE WAVE**

Now, perchance let’s assume the received signal is not directly in phase with signal generated at the receiver’s local oscillator mixer but is phase shifted with angle, $\phi$.

Multiplying the two we get,

$$
\left[ \sin (\omega t + \phi) \right] \times \left[ \sin (\omega t) \right] = \frac{e^{j\omega t} - e^{-j\omega t}}{j2} \times \frac{e^{j(\omega t + \phi)} - e^{-j(\omega t + \phi)}}{j2} \quad \ldots \ (32)
$$

$$
= \frac{e^{j(2\omega t + \phi)} - e^{j(\omega t - \omega t - \phi)} - e^{j(\omega t + \phi - \omega t)} + e^{-j(2\omega t + \phi)}}{-4} \quad \ldots \ (33)
$$

$$
= \frac{e^{j(2\omega t + \phi)} + e^{-j(2\omega t + \phi)}}{4} - \frac{e^{j\phi} - e^{-j\phi}}{4} \quad \ldots \ (34)
$$

$$
= \frac{1}{2} \left[ \frac{e^{j(2\omega t + \phi)} + e^{-j(2\omega t + \phi)}}{2} \right] - \frac{1}{2} \left[ \frac{e^{j\phi} - e^{-j\phi}}{2} \right] \quad \ldots \ (35)
$$

$$
= \left[ \frac{\cos \phi}{2} \right] - \frac{1}{2} \left[ \cos 2(\omega t + \phi) \right] \quad \ldots \ (36)
$$

Thus it can be seen that the high frequency signal, $\cos 2(\omega t + \phi)$, retains the phase shift, $\phi$, and that this phase shift also scales the D.C. offset value. Therefore, given a certain value of D.C. offset the value of $\phi$ can be mathematically calculated.

However, there is a limitation to be considered. $\Phi$ is limited to two quadrants only. A phase shift of $\pi/2$ cannot be distinguished from a phase shift of $-\pi/2$. To overcome this, the received signal is multiplied by both a sinusoidal waveform and a cosinusoidal waveform. Meaning that at the local oscillator mixer both sinusoidal and cosinusoidal waveforms should be generated.

**A COSINE WAVE AND A PHASEhifted SINE WAVE**

Mathematically, the output of a cosine local waveform and a phase shifted carrier sine wave is as follows

$$
\left[ \sin (\omega t + \phi) \right] \times \left[ \cos (\omega t) \right] = \frac{e^{j(\omega t + \phi)} - e^{-j(\omega t + \phi)}}{j2} \times \frac{e^{j\omega t} + e^{-j\omega t}}{2} \quad \ldots \ (37)
$$
Thus it can be seen that there is a scaling performed on the energy term as a result of phase shift. This minimises the received power in the signal and hence it is an undesired effect. In eliminating this effect, the phase shift term is maximized by either ensuring $\phi = 0^\circ$ for the cos term or $\phi = 90^\circ$ for the sin term. Secondly, it can be seen that a varying phase with time will produce a varying energy signal which is undesired for it can be a source of error in the decision process.

Due to this two effects as demonstrated above synchronisation becomes essential as it is a means of ensuring the frequency of the incoming signal is the same as that of the locally generated demodulating signal. It could be argued by making sure the transmitter frequency is the same as that of the receiver perfect synchronisation could be achieved but this is not the case. In the channel of transmission there are factors that affect the carrier frequency of the transmitted signal such as Doppler shift which would send the receiver out of synchronism with the incoming signal. Therefore, a method of synchronising the local oscillator with the incoming signal is pertinent.

2.2.3: SYNCHRONIZATION

Synchronization refers to the process of reproducing the local transmitter signal characteristics at the receiver end to ensure coherent demodulation and detection of the received modulated signal. This is essential as it is this reference signal that is compared with the incoming signal in order to make the maximum likelihood decision for accurate detection. When this is achieved the incoming carrier signal is said to be phase lock with the locally generated signal. In the afore discussions synchronization has been assumed. However, this is usually not the case.

[1] There are broadly three types of synchronization namely, phase and symbol synchronization and frame synchronization.

2.2.3.1: TYPES OF SYNCHRONIZATION

2.2.3.1.1: PHASE SYNCHRONIZATION

Phase synchronization as the name suggest refers to the process of ensuring as near perfect correspondence between the phase of the incoming carrier wave and the locally generated carrier. In the channel variations may take place. One such variation is the Doppler shift which is common in mobile radio communications. Doppler shift usually affects moving
receiver stations and appear to change the frequency of the received signal. This would be a source of errors in detection and would increase the bit error rate which is an undesirable effect.

2.2.3.1.2: SYMBOL SYNCHRONIZATION

Symbol synchronization helps to know the proper symbol integration interval – the interval over which energy is integrated prior to making symbol decision.

As a signal travels over some distance smearing of the signal because of attenuation. At some distance just next to the transmitter the signal shape may be as represented below. [1]

![Figure 13: A Digital signal representation at source](image)

Again at some distance away from the transmitter, say distance 4, due to degradation of the signal the signal is smeared out over a time interval. [1]

![Figure 14: Signal Degradation at some distance away from the source](image)

This makes it hard to determine the symbol length and it also causes inter-symbol interference (ISI) between successive symbols as both signals smear out over their given time and interfere. This affects the quality of detection and these effects must be taken into account. One method of addressing this matter is clock synchronization at the transmitter and receiver end. This is also known as symbol synchronization.

2.2.3.1.3: FRAME SYNCHRONIZATION

Frame synchronization is a higher form of synchronization which is done when information is arranged in some uniform blocks. This ensure that blocks of information are known. This is very important in consideration of error control coding where a message block is concatenated with error codes to form one long block of information. In decoding the
message signal all the code-word length is essential that it be known fully for accurate error correction and detection of the message signal.

2.2.3.2: CARRIER RECOVERY

In synchronization, an important matter is carrier recovery. Carrier recovery refers to the process obtaining the modulated signal carrier both in phase and frequency as it is this reference signal that will be mixed with incoming modulated signal in the demodulation process as discussed under the demodulation theory. A difference in frequency and phase between the incoming signal and locally generated demodulating carrier will be a source of error.

A basic circuit in carrier recovery is the phase locked loop, (PLL). This circuit not only aid in reproducing frequency and phase of the incoming carrier modulated signal but also aids in tracking the frequency and phase and achieve locking.

2.2.3.2.1: PHASE LOCK LOOP

The phase lock loop is the main component in this carrier recovery method. The basic concept of the phase lock loop is shown below. The basic circuit consists of three components. These are the phase detector, the loop filter and the voltage controlled oscillator. [1]

The phase detector compares the phase between the incoming signal, \( r(t) \) and the locally generated signal and produces the difference as \( e(t) \). As the error signal varies as the incoming signal and the locally generated signal vary in respect to each other the error signal varies. The loop filter is used to govern the response of the phase locked loop to these variations. This enables tracking of the signal. The Voltage Controlled Oscillator is the device that produces the carrier replica. The VCO is a device whose frequency of oscillation is controlled by the voltage value input into it.

Consider a normalized input signal \( r(t) \) as [1]

\[
r(t) = \cos \left[ \omega_c + \varphi(t) \right]
\]  

... (41)

where \( \omega_c \) is the nominal carrier frequency

\( \varphi(t) \) is the slowly varying phase with time
Similarly considering a VCO output of the form

\[ x(t) = -2 \sin [\omega_c t + \phi(t)] \]  

... (42)

The error signal produced will be

\[ e(t) = x(t) r(t) = 2 \sin [\omega_c t + \phi(t)] \cos [\omega_c t + \varphi(t)] \]  

... (43)

by geometric relations the equation above simplifies to

\[ e(t) = \sin [\phi(t) - \hat{\phi}(t)] + \sin [2\omega_c t + \varphi(t) + \hat{\phi}(t)] \]  

... (44)

with the small angle approximation \( \sin[\phi(t) - \hat{\phi}(t)] \approx [\phi(t) - \hat{\phi}(t)] \) it becomes

\[ e(t) = [\phi(t) - \hat{\phi}(t)] + \sin [2\omega_c t + \varphi(t) + \hat{\phi}(t)] \]  

... (45)

Given the loop filter is a low pass filter the double frequency term will be filtered out and the first term only of the equation will remain. This term will be the input of the VCO.

Assuming that the frequency \( \omega_c \) is the output frequency of the VCO when the phase difference is zero then the difference term in the frequency of the VCO can be expressed as the time differential of the phase term, \( \hat{\phi}(t) \).

\[ \Delta \omega(t) = \frac{d}{dt} [\hat{\phi}(t)] = K_0 y(t) \]  

... (46)

\[ \Delta \omega(t) = K_0 e(t) * f(t) \]  

... (47)

\[ \Delta \omega(t) = K_0 [\phi(t) - \hat{\phi}(t)] * f(t) \]  

... (48)

With \( K_0 \) defined as the gain of the VCO.

\( f(t) \) defined as the loop impulse response.

2.2.3.2.2: TRACKING

Tracking is the ability of the circuit to maintain synchronism with the changes in the incoming signal. Given that the two main features of a signal that can be altered during transmission namely, phase and frequency, tracking is therefore considered under these two features.

2.2.3.2.2.1: PHASE TRACKING

In demonstrating the tracking characteristics of the phase lock loop we consider a case where the phase of the input signal \( \varphi(t) \), is slowly varying with time.

If the phase difference \( [\varphi(t) - \hat{\phi}(t)] \) is positive, that is \( \varphi(t) > \hat{\phi}(t) \), then by appropriate choice of \( K_0 \) and \( f(t) \), the time derivative of \( \hat{\phi}(t) \) will be positive, so that \( \hat{\phi}(t) \) will increase with time, which will tend to reduce the magnitude of the difference \( [\varphi(t) - \hat{\phi}(t)] \).

On the other hand, if the phase difference is negative, \( \hat{\phi}(t) \) will decrease with time, which will also reduce the magnitude of the phase difference. Finally, if \( \varphi(t) = \hat{\phi}(t) \), then \( \hat{\phi}(t) \) will not change with time, and the equality will be maintained.
The Fourier transform of the equation (48)

\[ \Delta \omega(t) = K_o [\phi(t) - \dot{\phi}(t)] * f(t) \]

Is given as

\[ j\omega \dot{\phi}(\omega) = K_o [\phi(\omega) - \dot{\phi}(\omega)] F(\omega) \quad \text{... (49)} \]

rearranging the above we have

\[ \frac{\dot{\phi}(\omega)}{\phi(\omega)} = \frac{K_o F(\omega)}{j\omega + K_o F(\omega)} = H(\omega) \quad \text{... (50)} \]

Where \( H(\omega) \) is the closed loop transfer function of the PLL and the order is observed to be one more than the order of the loop filter.

Rearranging the equation again with our focus on the error term,

\[ E(\omega) = [\phi(\omega) - \dot{\phi}(\omega)] \quad \text{... (51)} \]

We have,

\[ E(\omega) = [1 - H(\omega)] \phi(\omega) \quad \text{... (52)} \]

\[ = \frac{j\omega\phi(\omega)}{j\omega + K_o F(\omega)} \quad \text{... (53)} \]

To obtain the steady state error characteristics of the system we use the final value theorem of the Fourier transform. The theorem states

\[ \lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} j\omega E(\omega) \quad \text{... (54)} \]

We have

\[ \lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} \frac{(j\omega)^2\phi(\omega)}{j\omega + K_o F(\omega)} \quad \text{... (55)} \]

Taking the case for a phase step function, the parameter \( \phi(\omega) \) is substituted by its Fourier transform which is taken as

\[ = \frac{\Delta \omega}{j\omega} \quad \text{... (56)} \]

The final theorem value then becomes

\[ \lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} \frac{(j\omega) \Delta \omega}{j\omega + K_o F(\omega)} = 0 \quad \text{... (57)} \]

Thus it can be seen for any offset value introduced into the network will be tracked by the loop and phase lock will be the steady state of the network.

2.2.3.2.2: FREQUENCY TRACKING

Since phase is the integral of frequency, the input phase will change linearly as a function of time for a constant input-frequency offset or a step frequency input. [1] Thus the
Fourier transform of the step frequency offset is the Fourier transform of the phase divided by $j\omega$.

$$\varphi(\omega) = \frac{\Delta\omega}{(j\omega)^2} \quad \ldots (58)$$

$\Delta\omega$ is defined as the magnitude of the frequency step.

Substituting in the final value theorem we get

$$\lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} \frac{\Delta\omega}{j\omega + K_0 F(\omega)} \quad \ldots (59)$$

Which simplifies into

$$= \frac{\Delta\omega}{K_0 F(\omega)} \quad \ldots (60)$$

Thus it can be seen that the steady state result is a function of the loop filter characteristics and the loop will track the input phase ramp, or frequency step, with a constant steady state error whose magnitude is dependent on the magnitude of the frequency step and the gain of the loop filter.

2.2.3.2.2.3: LINEARLY VARYING FREQUENCY/ FREQUENCY RAMP

Moreover, let us consider a frequency ramp, an input whose frequency is changing linearly with time. The Fourier transform of such an input is the integral of the frequency step and is given by;

$$\varphi(\omega) = \frac{\Delta\omega}{(j\omega)^3} \quad \ldots (61)$$

The steady state equation then simplifies to;

$$\lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} \frac{\Delta\omega/j\omega}{j\omega + K_0 F(\omega)} = \lim_{j\omega \to 0} \frac{\Delta\omega}{j\omega K_0 F(\omega)} \quad \ldots (62)$$

Which shows that the error for such a signal will be unbounded, tend to infinity.

A varying frequency input scenario, in light with the Doppler effect, corresponds to a moving accelerating receiver. This situation is common in day-to-day life and a way to overcome it is to introduce a second order PLL, where the loop filter is given by

$$F(\omega) = \frac{N(\omega)}{(j\omega)^2 D(\omega)} \quad \ldots (63)$$

where $N(\omega)$ is the numerator and $D(\omega)$ is the denominator.

Such that the final equation will be given by

$$\lim_{t \to \infty} e(t) = \lim_{j\omega \to 0} \frac{j\omega \Delta\omega}{K_0 N(\omega)} = 0 \quad \ldots (64)$$
2.2.3.2.3: SUPRESSED CARRIER LOOPS

Previously, all phase modulated communication systems used a system of design called the residual carrier component system where part of the energy was transmitted in the residual component carrier. This was seen to be in a sense wasted energy as it was not used in modulation and a shift was made from the system to the suppresses carrier system.

Nearly all modern BPSK the transmitters use supressed carrier systems where the average energy at carrier frequency is zero since all energy goes into modulation. However, this hinders tracking of the incoming signal as there is no energy in the carrier.

One method of going round this problem is through squaring of the BPSK signal which will yield a carrier related term at twice the frequency which can be tracked. This method is called the squaring loop. However, it has demerit of 'loop squaring loss' which serves to increases the complexity of the required demodulator circuit to overcome.

Also as a result of the interaction of data stream with the loop nonlinearities and the loop filter sidebands are produced in the spectrum that is input to the phase detector. These sidebands may contain stable frequencies that may produce a false lock on the system. The loop will be tracking a sideband frequency component and filtering out the real carrier.

2.2.3.2.4: THE COSTAS LOOP

Costas loop mainly finds its application in wireless receivers. [2] The Costas loop likewise deals with supressed carrier systems and serves to better the square loop by using two perfectly matched filters in its design. Below is the basic Costas loop circuit. [1]

![Costas Loop Circuit Diagram](image)

Figure 16: A basic Costas Loop circuit

The demodulated bit stream can be obtained through the indicated arrow, but essentially after any of the two filters. The demodulated stream is first taken through a threshold detector before the original message signal is reconstructed back and obtained from the receiver’s end whereas the circuit itself performs carrier recovery while eliminating the data signals.
2.2.3.2.4.1: PRINCIPLE OF OPERATION OF THE COSTAS LOOP

Suppose $s(t)$ represents a PSK modulated signal given by the relation

$$s_i(t) = \sqrt{2E} \cos (\omega t + \varphi) = \sqrt{2E} \left( \frac{e^{j(\omega t + \varphi)} + e^{-j(\omega t + \varphi)}}{2} \right) \quad \ldots (65)$$

Likewise suppose that the VCO generates a sine wave at certain frequency and phase given by the following relation.

$$x(t) = -2 \sin (\omega t + \hat{\varphi}) = -2 \left( \frac{e^{j(\omega t + \varphi)} - e^{-j(\omega t + \varphi)}}{j2} \right) \quad \ldots (66)$$

UPPER MIXER

In the upper mixer the two signals multiply as follows

$$s_i(t) * x_1(t) = -2 \left( \frac{e^{j(\omega t + \varphi)} + e^{-j(\omega t + \varphi)}}{2} \right) * \left( \frac{e^{j(\omega t - \varphi - \hat{\varphi})} - e^{-j(\omega t + \varphi)}}{j2} \right) \quad \ldots (67)$$

$$= -2 \left( \frac{e^{j(2\omega t + \varphi + \hat{\varphi})} - e^{-j(2\omega t + \varphi - \hat{\varphi})} + e^{j(\omega t - \varphi - \hat{\varphi})} - e^{-j(\omega t + \varphi)}}{j4} \right) \quad \ldots (68)$$

$$= -2 \left( \left( \frac{e^{j(2\omega t + \varphi + \hat{\varphi})} - e^{-j(2\omega t + \varphi - \hat{\varphi})}}{j4} \right) - \left( \frac{e^{j(\varphi - \hat{\varphi})} - e^{-j(\varphi - \hat{\varphi})}}{j4} \right) \right) \quad \ldots (69)$$

$$= - \left( \left( \sin (2\omega t + \varphi + \hat{\varphi}) - \sin (\varphi - \hat{\varphi}) \right) \right) \quad \ldots (70)$$

The low pass filter removes the high frequency component and the remaining term becomes

$$= \sin (\varphi - \hat{\varphi}) \quad \ldots (71)$$

$(\varphi - \hat{\varphi})$ is defined as the phase difference between the received message signal and the locally generated carrier.

LOWER MIXER

Likewise, in the lower mixer the following multiplication takes place where the locally generated carrier fed is now a cosine wave after the $90^\circ$ phase shift.
Let $x_2(t) = -2 \cos [\omega t + \hat{\phi}] = -2 \left( \frac{e^{j(\omega t + \phi)} + e^{-j(\omega t + \phi)}}{2} \right)$ ... (72)

Thus

$$s_1(t) * x_2(t) = -2 \left( \frac{e^{j(2\omega t + \phi + \hat{\phi})} + e^{-j(2\omega t + \phi + \hat{\phi})}}{4} \right) + \left( \frac{e^{j(\phi - \hat{\phi})} + e^{-j(\phi - \hat{\phi})}}{2} \right) \quad \ldots \quad (73)$$

$$= -2 \left( \frac{e^{j(2\omega t + \phi + \hat{\phi})} + e^{-j(2\omega t + \phi + \hat{\phi})}}{4} \right) + \left( \frac{e^{j(\phi - \hat{\phi})} + e^{-j(\phi - \hat{\phi})}}{2} \right) \quad \ldots \quad (74)$$

$$= - \left[ \left( \cos (2\omega t + \phi + \hat{\phi}) \right) - \cos (\phi - \hat{\phi}) \right] \quad \ldots \quad (75)$$

Through low pass filtering the high frequency component is eliminated and the remaining equation becomes

$$= \left[ \cos (\phi - \hat{\phi}) \right] \quad \ldots \quad (76)$$

$(\phi - \hat{\phi})$ is defined as the phase difference between the received message signal and the locally generated carrier.

**FINAL MIXER**

The two terms obtained after low pass filtering are again multiplied in the mixer before the VCO

$$= \left[ \sin (\phi - \hat{\phi}) \right] \ast \left[ \cos (\phi - \hat{\phi}) \right] \quad \ldots \quad (77)$$

$$= \left[ \sin (\phi - \hat{\phi}) \cos (\phi - \hat{\phi}) \right] \quad \ldots \quad (78)$$

which from the trigonometry yields the error term fed into the VCO to be

$$\frac{1}{2} \sin 2(\phi - \hat{\phi}) \quad \ldots \quad (79)$$

the equation becomes

$$\frac{1}{2} \sin 2(\phi - \hat{\phi}) \quad \ldots \quad (80)$$

This is the error signal driving the Costas loop VCO. As already shown in the Phase Lock Loop and Tracking sections this system can achieve phase lock hence carrier recovery.

The BPSK analysis of the Costas loop operation is just as is illustrated in the section above in the general principle of Costas loop operation.

However, BPSK Costas loop receiver requires accurate phase tracking which can present a complex design problem if the signals experience high Doppler rates or fading.
2.2.3.2.4.2: THE QPSK COSTAS LOOP

The conventional Costas loop QPSK demodulator takes the following form. [10]

![The Costas Loop of QPSK demodulator](image)

Figure 17: The Costas Loop of QPSK demodulator

The crossover arms are fitted with limiters which take the sign of the output of the arm filters and mixes it with that of the opposite arm. The limiters effectively demodulate the QPSK quadrature bits and the crossover produces a common phase-error term that is cancelled after subtraction. The subtraction leaves a remainder error term that is used to generate an error signal for phase control of the loop VCO, thereby closing the loop.

A hard limited Costas loop exhibits improved acquisition characteristics. It has a bandwidth of approximately the square of the Costas loop bandwidth thus allowing for acquisition of the frequency offset greater than the loop bandwidth. It also has an improved false lock performance. However, it suffers from the degradation of loop tracking jitters.

Given a QPSK signal takes the form

\[
S_{IJ}(t) = \pm I(t) \cos (\omega t + \varphi_1) \pm Q(t) \sin (\omega t + \varphi_2)
\]  

... (82)

Where the I(t) is the in-phase amplitude component of the QPSK signal while the Q(t) represents the quadrature amplitude component of the QPSK signal. However, these two will be ignored in the analysis as they offer little contribution the locking characteristics of the system.

In the upper mixer the incoming QPSK signal is multiplied with the following signal
\[ x(t) = -2 \sin [\omega t + \hat{\phi}] = -2 \left( \frac{e^{j(\omega t + \phi)} - e^{-j(\omega t + \phi)}}{j} \right) \]  

... (83)

since the QPSK signal has both the in-phase and quadrature parts both are multiplied by the locally generated wave.

THE UPPER ARM

The In-Phase component

From the equation (65 - 71) it can be seen that the In-phase, I(t), part of the QPSK signal becomes

\[ [\cos (\omega t + \varphi_1)] \ast [-2 \sin (\omega t + \hat{\phi})] \]

... (84)

\[ = - \left[ (\sin (2\omega t + \varphi_1 + \hat{\phi}) - \sin (\varphi_1 - \hat{\phi}) \right] \]

... (85)

\[ = (\sin (\varphi_1 - \hat{\phi})) \]

... (86)

\[ \] 

The quadrature Component

Likewise, the quadrature, Q(t), part of the same QPSK signal becomes

\[ [\sin (\omega t + \varphi_2)] \ast [-2 \sin (\omega t + \hat{\phi})] \]

... (87)

\[ = -2 \left[ \frac{e^{j(2\omega t + \varphi_2 + \varphi)} - e^{j(\omega t + \varphi_2 + \varphi)}}{-4} \right] \]

... (88)

\[ = \left[ \cos (2\omega t + \varphi_2 - \hat{\phi}) \right] - \left[ \cos (\varphi_2 - \hat{\phi}) \right] \]

... (90)

Through filtering the higher frequency components are eliminated and only the phase differences remain. Thus in the upper arm the resulting signal is

\[ = \sin(\varphi_1 - \hat{\phi}) - \cos(\varphi_2 - \hat{\phi}) \]

... (91)

THE LOWER ARM

The Quadrature Component

In the lower arm the same mixing takes place with the quadrature component represented by Q(t)

\[ [ \sin (\omega t + \varphi_2)] \ast [-2 \cos (\omega t + \hat{\phi})] \]

... (92)
Whose output after filtering can be seen from equation (85) to be

\[ \sin(\varphi_2 - \hat{\varphi}) \]

**The In-Phase Component**

Likewise, the in-phase component represented by the I(t) yields

\[
\begin{align*}
&[\cos(\omega t + \varphi_1)] \times [-2 \cos(\omega t + \hat{\varphi})] \\
&\text{... (93)} \\
&= -2 \left[ \frac{e^{j(\omega t + \varphi_1)} + e^{-j(\omega t + \varphi_1)}}{2} \times \frac{e^{j(\omega t + \hat{\varphi})} + e^{-j(\omega t + \hat{\varphi})}}{2} \right] \\
&\text{... (94)} \\
&= -2 \left[ \frac{e^{j(2\omega t + \varphi_1 + \hat{\varphi})} + e^{-j(2\omega t + \varphi_1 + \hat{\varphi})}}{4} + \frac{e^{j(\varphi_1 - \hat{\varphi})} + e^{-j(\varphi_1 - \hat{\varphi})}}{4} \right] \\
&\text{... (95)} \\
&= - \left[ \cos(\varphi_1 - \hat{\varphi}) \right] - \left[ \cos(2\omega t + \varphi_1 - \hat{\varphi}) \right] \\
&\text{... (96)}
\end{align*}
\]

Which after filtering simplifies to

\[ - \left[ \cos(\varphi_1 - \hat{\varphi}) \right] \]

\[ \text{... (97)} \]

Thus the total lower arm output is

\[ \left[ \sin(\varphi_2 - \hat{\varphi}) \right] - \left[ \cos(\varphi_1 - \hat{\varphi}) \right] \]

\[ \text{... (98)} \]

**THE CROSS ARM MIXERS**

Equations (91) and (98) are multiplied together in the mixers before the summer block. Given that they are symmetrical mixers the analysis of one will also serve to illustrate that of the other

Letting \((\varphi_1 - \hat{\varphi})\) be represented by \(\Delta \Psi_1\)

And \((\varphi_2 - \hat{\varphi})\) be represented by \(\Delta \Psi_2\)

\[ \left[ \sin \Delta \Psi_1 \cos \Delta \Psi_2 \right] \times \left[ \sin \Delta \Psi_2 \cos \Delta \Psi_1 \right] \]

\[ \text{... (99)} \]

\[ \sin \Delta \Psi_1 \sin \Delta \Psi_2 \cos \Delta \Psi_1 \cos \Delta \Psi_2 \sin \Delta \Psi_2 \cos \Delta \Psi_2 \cos \Delta \Psi_1 \]

\[ \text{... (100)} \]

By trigonometry

\[ \cos \Delta \Psi_2 \cos \Delta \Psi_1 + \sin \Delta \Psi_1 \sin \Delta \Psi_2 = \cos(\Delta \Psi_1 - \Delta \Psi_2) = \cos(\varphi_1 - \varphi_2) \]

\[ \sin \Delta \Psi_1 \cos \Delta \Psi_1 = \frac{1}{2} \sin 2\Delta \Psi_1 \quad ; \quad \cos \Delta \Psi_2 \sin \Delta \Psi_2 = \frac{1}{2} \sin 2\Delta \Psi_2 \]
\[ = \cos(\varphi_1 - \varphi_2) - \left( \frac{1}{2} \sin 2\Delta\psi_1 + \frac{1}{2} \sin 2\Delta\psi_2 \right) \quad \ldots \text{(101)} \]

**THE SUMMER**

In the summer the two symmetric signal add up and the output is given by

\[ = \cos(\varphi_1 - \varphi_2) - \left[ (\sin (2\varphi_1 - 2\hat{\varphi}) + \sin (2\varphi_2 - 2\hat{\varphi}) \right] \quad \ldots \text{(102)} \]

\[ = \cos(\varphi_1 - \varphi_2) - \left[ (\sin (2\varphi_1 - 2\hat{\varphi}) + \sin (2\varphi_2 - 2\hat{\varphi}) \right] \quad \ldots \text{(103)} \]

Equation (103) is the error term. This is also the VCO’s driving voltage.

It should be noted that the error term has a constant to it. This constant is the value to which the input of the VCO will be approaching when the phase difference is approaching zero. This will be an offset value which can also be termed as the steady state error of the phase lock loop. The phase lock loop will track the carrier with the constant steady state error term.

The maximum steady state error is seen to be 1 from equation (103) and it is obtained when the phase difference is zero between the incoming signal and locally generated carrier since the value of \( \varphi_1, \varphi_2 \) are either 0, 180.

**2.2.3.2.5: THE REMODULATOR**

Re-modulation is another method of carrier recovery. The transmitted data after demodulation is again modulated by the carriers produced by the locally (by the VCO) and the resultant signal mixed with the incoming signal taken through the loop filter and the phase difference fed into the VCO. The product of such a mixing removes all modulation. The PLL therefore tracks the incoming carrier.

The re-modulator achieves carrier recovery at frequencies less than IF hence allow hardware realization. This results in a low cost demodulator [3]. Compared to the Costas loop the re-modulator has a faster acquisition time, that is, achieves phase lock faster. [2]

**2.2.3.2.5.1: A BPSK REMODULATOR LOOP**

A basic BPSK re-modulator circuit is given below. [10]
**ANALYSIS**

Consider the carrier of a BSPK incoming signal given by the equation (65)

\[ s_i(t) = \cos [\omega t + \varphi] = \left( \frac{e^{j(\omega t + \varphi)} + e^{-j(\omega t + \varphi)}}{2} \right) \]

At the mixer the signal is multiplied by the local carrier generated by the VCO, which is at a given phase offset with reference to the BPSK signal

\[ x(t) = \sin [\omega t + \hat{\varphi}] \]  

... (104)

the product of the two from equation (65 - 71) can be seen to be

\[ s_i(t) \ast x(t) = \frac{1}{2} [\sin (\varphi - \hat{\varphi})] - \frac{1}{2} (\sin (2\omega t + \varphi + \hat{\varphi})) \]

... (105)

After filtering the double frequency term is eliminated and the signal degenerates into

\[ \frac{1}{2} [\sin (\varphi - \hat{\varphi})] \]

... (106)

At the mixer this signal is multiplied with the cosine term of the locally generated carrier.

\[ \frac{1}{2} [\sin (\varphi - \hat{\varphi})] \ast \cos [\omega t + \hat{\varphi}] \]

... (107)

Given

\[ \sin (\varphi - \hat{\varphi}) = \frac{e^{j(\varphi - \hat{\varphi})} - e^{-j(\varphi - \hat{\varphi})}}{j2} \]

... (108)

And
\[
\cos [\omega t + \phi] = \frac{e^{j(\omega t + \phi)} + e^{-j(\omega t + \phi)}}{2} \quad \text{... (109)}
\]

Equation (107) becomes

\[
\frac{1}{2} \left[ \sin (\varphi - \bar{\phi}) \right] * \cos [\omega t + \bar{\phi}]
\]

\[
= \frac{1}{2} \left[ \frac{e^{j(\varphi - \bar{\phi})} - e^{-j(\varphi - \bar{\phi})}}{j2} \right] \quad \text{... (110)}
\]

\[
\frac{1}{2} \left[ \frac{e^{j(\omega t + \varphi)} + e^{-j(\omega t + \varphi)} - e^{j(\omega t + 2\varphi - \varphi)} - e^{-j(\omega t + 2\varphi - \varphi)}}{j4} \right]
\]

\[
= \frac{1}{4} \left[ \frac{e^{j(\omega t + \varphi)} - e^{-j(\omega t + \varphi)}}{j2} \right] - \frac{1}{4} \left[ \frac{e^{j(\omega t + 2\varphi - \varphi)} - e^{-j(\omega t + 2\varphi - \varphi)}}{j2} \right] \quad \text{... (111)}
\]

\[
= \frac{1}{4} \sin (\omega t + \varphi) - \frac{1}{4} \sin (\omega t + 2\bar{\phi} - \varphi) \quad \text{... (112)}
\]

In the next mixer the signal in equation (112) is multiplied with the incoming signal and the product fed into the loop filter and the error term is used to drive the VCO.

\[
\left[ \frac{1}{4} \sin (\omega t + \varphi) - \frac{1}{4} \sin (\omega t + 2\bar{\phi} - \varphi) \right] * \cos [\omega t + \bar{\phi}] \quad \text{... (113)}
\]

For better illustrative purposes the multiplication is carried out in two parts

1. \[
\frac{1}{4} \sin (\omega t + \varphi) * \cos [\omega t + \bar{\phi}] \quad \text{... (114)}
\]

2. \[
\frac{1}{4} \sin (\omega t + 2\bar{\phi} - \varphi) * \cos [\omega t + \bar{\phi}] \quad \text{... (115)}
\]

The first part

1. \[
\frac{1}{4} \sin (\omega t + \varphi) * \cos [\omega t + \bar{\phi}]
\]

\[
= \frac{1}{4} \left[ \frac{e^{j(\omega t + \varphi)} - e^{-j(\omega t + \varphi)}}{j2} \right] \quad \text{... (117)}
\]

\[
= \frac{1}{4} \left[ \frac{e^{j(2\omega t + 2\varphi)} + e^{j(0)} - e^{-j(0)} - e^{-j(2\omega t + 2\varphi)}}{j4} \right] \quad \text{... (118)}
\]

\[
= \frac{1}{8} \frac{e^{j(2\omega t + 2\varphi)} - e^{-j(2\omega t + 2\varphi)}}{j2} \quad \text{... (119)}
\]

\[
= \frac{1}{8} \sin (2\omega t + 2\varphi) \quad \text{... (120)}
\]
The second part

2. \( \frac{1}{4} \sin (\omega t + 2\phi - \varphi) \cos (\omega t + \varphi) \)

\[
\frac{1}{4} \left[ e^{j(\omega t + 2\phi - \varphi)} - e^{-j(\omega t + 2\phi - \varphi)} \right] \ast \frac{e^{j(\omega t + \varphi)} + e^{-j(\omega t + \varphi)}}{2} = \frac{1}{4} \left[ e^{j(\omega t + 2\phi)} + e^{-j(\omega t + 2\phi)} \right] \quad \text{(121)}
\]

\[
= \frac{1}{4} \left[ \frac{e^{j(2\omega t + 2\phi)} + e^{-j(2\omega t + 2\phi)}}{j4} \right] = \frac{1}{8} \left[ e^{-j(2\omega t + 2\phi) - e^{-j(2\omega t - 2\phi)}} \right] = \frac{1}{8} \left[ e^{j(2\phi - 2\varphi)} - e^{-j(2\phi - 2\varphi)} \right] \quad \text{(122)}
\]

\[
= \frac{1}{8} \left[ \frac{e^{j(2\omega t + 2\phi)} - e^{-j(2\omega t + 2\phi)}}{j2} \right] = \frac{1}{8} \left[ e^{j(2\phi - 2\varphi)} + e^{-j(2\phi - 2\varphi)} \right] \quad \text{(123)}
\]

\[
= \frac{1}{8} \sin (2\omega t + 2\phi) + \frac{1}{8} \sin (2\varphi - 2\phi) \quad \text{(124)}
\]

Thus from the solution in equation (120) it can be seen that the term has a double frequency term and will be filtered out in the phase lock loop filter. Likewise, the first part of the equation (124) will filtered and the VCO error driving voltage will be seen to be

\[
\frac{1}{8} \sin (2\varphi - 2\varphi) \quad \text{(125)}
\]

This system as shown in the phase lock loop analysis is seen to achieve phase lock when an incoming carrier of a slightly shifted phase is input into it with reference to its locally generated carriers.

2.2.3.2.5.2: A QPSK REMODULATOR LOOP

A QPSK re-modulator loop is very similar to that of a BPSK given the a QPSK signal consists of two BPSK signals that are modulated simultaneously with carriers at quadrature. Given below is an illustration of the QPSK re-modulator loop circuit. [6]
ANALYSIS

Consider a QPSK signal given in equation (82).

\[ S_I(t) = \pm I(t) \cos (\omega t + \varphi_1) \pm Q(t) \sin (\omega t + \varphi_2) \]

It has both the in-phase bits and quadrature bits encoded in the in-phase carrier and the quadrature carrier. The carrier recovery system also has two arms that aid in demodulating each and a re-modulation section where the bits are re-modulated and added back to form a QPSK signal which is then mixed with the original incoming signal and the error term after filtering used to drive the VCO so as to achieve phase and frequency lock.

Considering only the frequency and phase components the incoming QPSK signal is multiplied by the locally generated carrier at a given frequency and phase, \( \sin [\omega t + \hat{\varphi}] \)

UPPER ARM ANALYSIS

The general signal multiplication that takes place in the first mixer is given by the following

\[ [\cos (\omega t + \varphi_1) + \sin (\omega t + \varphi_2)] * [\sin (\omega t + \hat{\varphi})] \]  ... (126)

Taking the cos part and multiplying it by the sine part

\[
\cos (\omega t + \varphi_1) * \sin (\omega t + \hat{\varphi}) = \frac{e^{j(\omega t + \varphi_1)} + e^{-j(\omega t + \varphi_1)}}{2} * \frac{e^{j(\omega t + \hat{\varphi})} - e^{-j(\omega t + \hat{\varphi})}}{j2} \]  ... (127)

\[
= \frac{e^{j(2\omega t + \varphi_1 + \hat{\varphi})} - e^{j(\omega t - \omega t + \varphi_1 - \hat{\varphi})} + e^{j(\omega t - \omega t + \varphi_1 - \hat{\varphi})} - e^{j(2\omega t + \varphi_1 + \hat{\varphi})}}{j4}
\]

\[
= \frac{1}{2} \left[ e^{j(2\omega t + \varphi_1 + \hat{\varphi})} + e^{-j(2\omega t + \varphi_1 + \hat{\varphi})} \right] - \frac{1}{2} \left[ e^{j(\varphi_1 - \hat{\varphi})} + e^{-j(\varphi_1 - \hat{\varphi})} \right] \]  ... (128)

\[
= \frac{1}{2} \sin (2\omega t + \varphi_1 + \hat{\varphi}) - \frac{1}{2} \sin (\varphi_1 - \hat{\varphi}) \]  ... (129)

Similarly, taking the sine part and multiplying it by the sine part

\[
\sin (\omega t + \varphi_2) * \sin (\omega t + \hat{\varphi}) = \frac{e^{j(\omega t + \varphi_2)} - e^{-j(\omega t + \varphi_2)}}{j2} * \frac{e^{j(\omega t + \hat{\varphi})} - e^{-j(\omega t + \hat{\varphi})}}{j2} \]  ... (130)

\[
= \frac{e^{j(2\omega t + \varphi_2 + \hat{\varphi})} - e^{j(\omega t - \omega t + \varphi_2 - \hat{\varphi})} - e^{j(\omega t - \omega t + \varphi_2 - \hat{\varphi})} + e^{j(2\omega t + \varphi_2 + \hat{\varphi})}}{-4}
\]

\[
= \frac{1}{2} \left[ e^{j(2\omega t + \varphi_2 + \hat{\varphi})} + e^{-j(2\omega t + \varphi_2 + \hat{\varphi})} \right] - \frac{1}{2} \left[ e^{j(\varphi_2 - \hat{\varphi})} + e^{-j(\varphi_2 - \hat{\varphi})} \right] \]  ... (131)

\[
= -\frac{1}{2} \cos (2\omega t + \varphi_2 + \hat{\varphi}) + \frac{1}{2} \cos (\varphi_2 - \hat{\varphi}) \]  ... (132)

Through the appropriate filtering the double frequency terms in equation (129) and (132) are filtered and the resultant signal in the upper arm is given by
\[
\frac{1}{2} \cos (\varphi - \hat{\varphi}) - \frac{1}{2} \sin (\varphi - \hat{\varphi}) \quad \ldots \quad (133)
\]

In this modulation scheme the original in-phase modulated bit stream is here obtained through appropriate gain addition and saturation to get the modulated message signal. (Since the bit information is contained in the phase shift \( \varphi \).) This message signal is bipolar and is used in the re-modulation process.

Through modulation equations the equation of the re-modulated waveform will be given by

\[
\cos (\omega t + \hat{\varphi}_2) \quad \ldots \quad (134)
\]

**LOWER ARM ANALYSIS**

\[
[\cos (\omega t + \varphi_1) + \sin (\omega t + \varphi_2)] * [\cos (\omega t + \hat{\varphi})]
\]

Taking the cos part of the QPSK signal and multiplying it by the cosine part of the locally generated carrier

\[
\cos (\omega t + \varphi_1) * \cos (\omega t + \hat{\varphi}) = \frac{e^{j(\omega t + \varphi_1) + e^{-j(\omega t + \varphi_1)}}}{2} * \frac{e^{j(\omega t + \hat{\varphi}) + e^{-j(\omega t + \hat{\varphi})}}}{2} \quad \ldots \quad (135)
\]

\[
= \frac{1}{4} \left[ e^{j(2\omega t + \varphi_1 + \varphi) + e^{-j(2\omega t + \varphi_1 + \varphi)}} \right] + \frac{1}{2} \left[ e^{j(\varphi_1 - \hat{\varphi}) + e^{-j(\varphi_1 - \hat{\varphi})}} \right] \quad \ldots \quad (136)
\]

\[
= \frac{1}{2} \cos (2\omega t + \varphi_1 + \hat{\varphi}) + \frac{1}{2} \cos (\varphi_1 - \hat{\varphi}) \quad \ldots \quad (137)
\]

Taking the sine part of the QPSK signal and multiplying it by the cosine part of the locally generated carrier

\[
\sin (\omega t + \varphi_2) * \cos (\omega t + \hat{\varphi}) = \frac{e^{j(\omega t + \varphi_2) - e^{-j(\omega t + \varphi_2)}}}{j2} * \frac{e^{j(\omega t + \hat{\varphi}) + e^{-j(\omega t + \hat{\varphi})}}}{2} \quad \ldots \quad (138)
\]

\[
= \frac{1}{4} \left[ e^{j(2\omega t + \varphi_2 + \varphi) - e^{-j(2\omega t + \varphi_2 + \varphi)}} \right] + \frac{1}{2} \left[ e^{j(\varphi_2 - \hat{\varphi}) - e^{-j(\varphi_2 - \hat{\varphi})}} \right] \quad \ldots \quad (139)
\]

\[
= \frac{1}{2} \sin (2\omega t + \varphi_2 + \hat{\varphi}) + \frac{1}{2} \sin (\varphi_2 - \hat{\varphi}) \quad \ldots \quad (140)
\]

Through the appropriate filtering the double frequency terms in equation (143) and (146) are filtered and the resultant signal in the lower arm is given by

\[
\frac{1}{2} \cos (\varphi_1 - \hat{\varphi}) + \frac{1}{2} \sin (\varphi_2 - \hat{\varphi}) \quad \ldots \quad (141)
\]
By similar signal processing as in the upper arm the quadrature bit stream is recovered in bipolar form. The recovered message signal is used to re-modulate the locally generated carrier.

The resultant equation is given by

$$\sin(\omega t + \hat{\varphi}_1)$$ ... (142)

At the summer on the far right the two re-modulated BPSK signals, equation (134) and (142) add up to form a QPSK signal given by the following relation. (It is the phase that is of interest as it contains the information as well as the frequency component)

$$= \cos(\omega t + \hat{\varphi}_2) + \sin(\omega t + \hat{\varphi}_1)$$ ... (143)

Following, at the multiplier this locally generated QPSK signal, equation (143), is multiplied by the incoming QPSK signal, equation (82), which is time delayed to take care of the delay introduced by the circuitry.

The multiplication is as shown below.

$$\left[\cos(\omega t + \varphi_1) + \sin(\omega t + \varphi_2)\right] \times \left[\cos(\omega t + \hat{\varphi}_2) + \sin(\omega t + \hat{\varphi}_1)\right]$$ ... (144)

The multiplication is carried out in four parts.

1.) \(\cos(\omega t + \varphi_1) \times \cos(\omega t + \hat{\varphi}_2)\)
2.) \(\cos(\omega t + \varphi_1) \times \sin(\omega t + \hat{\varphi}_1)\)
3.) \(\sin(\omega t + \varphi_2) \times \cos(\omega t + \hat{\varphi}_2)\)
4.) \(\sin(\omega t + \varphi_2) \times \sin(\omega t + \hat{\varphi}_1)\)

Part (1) based on the analysis done in equations (135) to (137) is seen to yield

$$=\frac{1}{2} \cos(2\omega t + \varphi_1 + \hat{\varphi}_2) + \frac{1}{2} \cos(\varphi_1 - \hat{\varphi}_2)$$ ... (145)

Part (2) based on the analysis done in equations (127) to (129) is seen to yield

$$=\frac{1}{2} \sin(2\omega t + \varphi_1 + \hat{\varphi}_1) - \frac{1}{2} \sin(\varphi_1 - \hat{\varphi}_1)$$ ... (146)

Part (3) based on the analysis done in equations (138) to (140) is seen to yield

$$=\frac{1}{2} \sin(2\omega t + \varphi_2 + \hat{\varphi}_2) + \frac{1}{2} \sin(\varphi_2 - \hat{\varphi}_2)$$ ... (147)

Part (4) based on the analysis done in equations (130) to (132) is seen to yield

$$=\frac{1}{2} \cos(2\omega t + \varphi_2 - \hat{\varphi}_1) + \frac{1}{2} \cos(\varphi_2 - \hat{\varphi}_1)$$ ... (148)

After low pass filtering to remove the double frequency components and summing up the results of equations (145-148) yields
\[
\frac{1}{2} \cos (\varphi_1 - \hat{\varphi}_2) + \frac{1}{2} \cos (\varphi_2 - \hat{\varphi}_1) + \frac{1}{2} \sin (\varphi_2 - \hat{\varphi}_2) - \frac{1}{2} \sin (\varphi_1 - \hat{\varphi}_1)
\]

This is the error term into the VCO. It has a constant value of 1 in QPSK systems. By designing an appropriate loop filter transfer function the error term can be made to go to zero as time increases.
3.1: INTRODUCTION

In the achievement of the project objectives the Mat lab simulation software was used. Mat lab software can be considered to consist of two part; the Mat lab workspace and Simulink. Mat lab work space primarily does simulation through the input of relevant codes while Simulink provides blocks and some electrical components in block from which aids in the visualization of the system as well as enhance understanding and presentation. For this reason, Simulink was used in the undertaking of the design of the carrier recovery system.

3.2: GENERAL SYSTEM DESIGN

With the project objective to design and demonstrate carrier recovery by remodulation a QPSK modem was constructed and carrier recovery by both Costas loop and remodulation illustrated and compared. The Simulink QPSK block was avoided as the carrier frequency used to generate the QPSK signal could not be varied from the QPSK block properties and hence demonstration of the phase tracking characteristics could not be observed and consequently carrier recovery at different frequencies. The design was thus based on a block to block model.

A general modulator-demodulator design was made using sub-systems designs as follows

![A QPSK Based Carrier Recovery System](image)

Figure 20: The General Carrier Recovery System

On the demodulation and detection end we had the following blocks:

1. Low pass filter
2. A 90° phase shifter
3. A voltage controlled oscillator/the receiver’s local carrier generator
3.2.1: THE QPSK MODULATOR DESIGN

Inside the QPSK modulator block of the modem we had the following main blocks:

1. The data and clock source.
2. The serial to parallel converter.
3. The unipolar to bipolar converter
4. The local transmitter carrier generators
5. The multipliers
6. Adders

The aim of the modulator section is to generate a QPSK modulated message signal for transmission over a channel. Given below are the main blocks found in the QPSK modulator block.

3.2.1.1: THE DATA AND CLOCK SOURCE.

Two block were used inside this sub-system, namely; the binary generator and the clock. The binary generator provided a simulation of the data signal to be used in the experiment while the clock provided the signal to be used in clocking the D flip flops used in the serial to parallel converter.
3.2.1.1: THE BINARY GENERATOR

The binary generator is a block that gives digital signal as it output. A sequence of 1’s and 0’s. This sequence is randomly generated and forms a serial stream of data signals that will be used as the modulating signal. The produced stream of data signals is what we want to transmit over a channel after the appropriate modulation technique and finally obtain back after demodulation of the signal. Such a signal is what is expected from the generator.

![Digital output of binary generator](image)

**Figure 22: Digital output of binary generator**

In effecting of this the Bernoulli binary generator found in Simulink library under Communication system toolbox, under communication sources, under random data sources was used. A display of the generated signal was made in the results section. Below is the Bernoulli binary generator block and its associated properties that were used.

![Bernoulli Binary Generator](image)

**Figure 23: Bernoulli Binary Generator**

Below are the Bernoulli block parameters as used in the set up.

<table>
<thead>
<tr>
<th>BERNOULLI BINARY GENERATOR BLOCK</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Probability of a zero</td>
<td>0.5</td>
</tr>
<tr>
<td>Initial seed</td>
<td>41</td>
</tr>
<tr>
<td>Sample time</td>
<td>0.025</td>
</tr>
<tr>
<td>Output data type</td>
<td>Double</td>
</tr>
</tbody>
</table>

Table 2: Bernoulli Binary Generator Parameters
### 3.2.1.1.2: THE CLOCK SOURCE

A clock block is used to pulse the flip flops to enable them to transit from one state to the next. It is obtained in the Simulink library under Sim Extras, under Flip flops section. Below is the representation of the clock block in Simulink and its associated properties.

![Clock Block](image)

**Figure 24: A clock block**

<table>
<thead>
<tr>
<th>CLOCK BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value</td>
</tr>
<tr>
<td>Period</td>
</tr>
</tbody>
</table>

**Table 3: Clock Block Parameters**

### 3.2.1.2: THE SERIAL TO PARALLEL CONVERTER

For a BPSK modulation technique each data signal would be modulated at a given time interval. However, for the QPSK modulation technique the serial data signal is taken to be a di-bit and hence in the same given time interval two data signal are modulated on the different arms of the modulating section, either the in-phase or the quadrature arm. Thus it can be seen that QPSK has twice the bit rate as BPSK.

To generate this two signals that are to be modulated within the same given time interval the stream is considered to a di-bit, only theoretically, then each two data signals converted from serial to parallel, for parallel processing(modulation) of the signal.

The serial to parallel converter was designed through basic electronic components, such as AND gate, NOT gate and the D-flip flops. The following is the expected output of the serial to parallel converter. [5]
In Simulink, these was effected through various blocks found in the software. These are:

1. D flip-flops which are found in the Simulink library under Simulink extras then under flip flops. The D flip flops truth table is given below. [6]

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>D INPUT</th>
<th>Q OUTPUT</th>
<th>! Q OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>! Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Q</td>
<td>! Q</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 4: D-Flip Flop States

Simply illustrating that when the flip flop is clocked the input at the D-input is seen at the Q-output. Below is the Simulink model of the D flip flop.

2. The logic AND gate is found under commonly used blocks. With appropriate alteration of the properties of the AND block the NOT block is obtained. Given below is the Simulink representations of the NOT gate with its associated truth table.
Table 5: NOT gate Operation

<table>
<thead>
<tr>
<th>Operation</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 6: AND Block parameters

<table>
<thead>
<tr>
<th>AND BLOCK PROPERTIES</th>
<th>Operation</th>
<th>Number of inputs</th>
<th>Output data types</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NOT</td>
<td>2</td>
<td>Boolean</td>
</tr>
</tbody>
</table>

Below is the AND gate with its respective truth table and block properties

Table 7: AND gate Operation

<table>
<thead>
<tr>
<th>AND GATE</th>
<th>INPUT A</th>
<th>INPUT B</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AND BLOCK PROPERTIES</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------------------</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Operation</strong></td>
<td>AND</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Number of inputs</strong></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output data type</strong></td>
<td>Boolean</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 8: AND Block Parameters

3. The terminator block is also obtained from the commonly used block section. The terminator aids in closing open connections in the system. Below is the Simulink representation.

![Terminator Block](image)

**Figure 29: A terminator block**

4. The constant block is used to feed a constant value into the various blocks used in design. In this given design it used to feed a value into the flip flops used. Below is its Simulink representation and block parameters. Like the terminator block it is found under the commonly used block in the Simulink library.

![Constant Block](image)

**Figure 30: A constant block**

<table>
<thead>
<tr>
<th>CONSTANT BLOCK PROPERTIES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Constant value</strong></td>
</tr>
<tr>
<td><strong>Sample time</strong></td>
</tr>
<tr>
<td><strong>Output minimum</strong></td>
</tr>
<tr>
<td><strong>Output maximum</strong></td>
</tr>
<tr>
<td><strong>Output data type</strong></td>
</tr>
</tbody>
</table>

Table 9: Constant Block Parameters

5. The data type conversion block converts the input data received on the input side to the specified output data type. It is found in the Simulink library under the
commonly used blocks section. Below is its Simulink representation and the block parameters.

![Data Type Conversion Block](image)

**Figure 31: Data type conversion block**

<table>
<thead>
<tr>
<th>DATA TYPE CONVERSION BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Input to output to have equal</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

**Table 10: Data Type Conversion Block Parameters**

The above described components were designed in a manner to effect a serial to parallel converter to the incoming data bit stream. (assumed a di-bit data stream). The design that achieved the serial to parallel converter is given below.

![Serial to Parallel Converter](image)

**Figure 32: Serial to Parallel Converter circuit**
3.2.1.3: THE UNIPOLAR TO BIPOLAR CONVERTER

The generated bit stream from the Bernoulli generator is a return to zero signal, that is, higher voltage is used to represent the 1 bits and zero voltage is used to represent the 0 bits. This is incompatible with the QPSK modulation scheme as the symbol energy is QPSK are either positive or negative as can be seen from the di-bit table.

The unipolar converter hence serves to convert a unipolar, a single sided signal, to a bipolar, double sided signal. Whereas the unipolar had the 1’s represent by a positive signal and the 0’s represented by zero signal the bipolar has the 1’s represented by a positive signal and the 0’s represented by a negative signal of equal magnitude.

To effect this in Simulink simple mathematical procedures were used to achieve it through the use of constant blocks, a product block and an addition block. Below is the diagrammatic representation of the unipolar to bipolar converters through the use of the above mentioned blocks.

![Diagram](image)

Figure 33: Unipolar to Bipolar configuration

The input to the product block is multiplied by two, if it is a 1 it is doubled to become 2 if it is a 0 it retains its value. The product from the block is then added to -1, if it is a 2 it becomes 1, if it is a 0 it becomes -1. Thus it can be seen that the above configuration effects the unipolar to bipolar converter as an input of 1 gives an output of 1 and input of 0 gives and output of -1.

Thus the block parameters as used are given below.

<table>
<thead>
<tr>
<th>CONSTANT 2 BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant value</td>
</tr>
<tr>
<td>Sample time</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
</tbody>
</table>

Table 11: Constant Block 2 Parameters

43
<table>
<thead>
<tr>
<th>CONSTANT 1 BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant value</td>
</tr>
<tr>
<td>Sample time</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
</tbody>
</table>

Table 12: Constant Block 1 Parameters

<table>
<thead>
<tr>
<th>PRODUCT BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs</td>
</tr>
<tr>
<td>Multiplication</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

Table 13: Product Block Parameters

<table>
<thead>
<tr>
<th>ADD BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs</td>
</tr>
<tr>
<td>List if signs</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

Table 14: Add Block Parameters

3.2.1.4: CARRIER GENERATORS

A single sine wave generator block could not be used to generate the required frequencies of the carrier. At high frequencies the output of the block was triangular wave as opposed to a smooth sine wave. This was due to limitations in the Mat lab program.

In an attempt to reproduce with good accuracy, the desired carrier signals, a discrete sine wave block was used. A sampled sine wave was used. However, the sampling time was so set that the output mirrored a smooth sine wave.
Below is the given configuration of the carrier generators.

![Carrier Generators Diagram]

Figure 34: Carrier generators configuration

The parameters for sine wave block 1 was set as with a 0° initial phase shift whereas that of block 2 was set with a 90° phase shift.

This set up was put under a block titled “subsystem 3 = Carrier generators”.

![Carrier Generator Block Diagram]

Figure 35: Carrier Generator Block

This set up was used to both generate sine and cosine carriers as can be seen.

Below are the chosen parameters of the aforementioned blocks.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude</td>
<td>1</td>
</tr>
<tr>
<td>Frequency</td>
<td>120</td>
</tr>
<tr>
<td>Phase offset</td>
<td>0, 90</td>
</tr>
<tr>
<td>Sample mode</td>
<td>Discrete</td>
</tr>
<tr>
<td>Output complexity</td>
<td>Real</td>
</tr>
<tr>
<td>Computational method</td>
<td>Trigonometric</td>
</tr>
<tr>
<td>----------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>Sample time</td>
<td>1/10000</td>
</tr>
<tr>
<td>Samples per Frame</td>
<td>1</td>
</tr>
<tr>
<td>Output data type</td>
<td>Double</td>
</tr>
</tbody>
</table>

Table 15: Discrete Sine wave Block Parameters

### 3.2.1.5: MIXERS AND MULTIPLIERS

In the modulator end we have two of these blocks. They serve to multiply two or more signals inputs fed into them. In the configuration they are used to multiply the digital bipolar signal with the generated carrier to give out the PSK modulated signal which will be transmitted. Two of these blocks are used as for in the case of QPSK modulation takes place in two arms. The in-phase and quadrature arms. The modulation of each arm is then brought and added together for transmission.

Below is the diagrammatic representation of the product blocks.

![Product block diagram](image)

**Figure 36: Product block**

The following are the block parameters that were used in the set up.

<table>
<thead>
<tr>
<th>PRODUCT BLOCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs</td>
</tr>
<tr>
<td>Multiplication</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

Table 16: Product Block Parameters

The adder block is used to sum all the PSK generated signal together with the Additive White Gaussian noise signal. This is the final signal processing in the modulation scheme before transmission.
Below is the adder block diagrammatic representation

![Adder Block Diagram](image)

**Figure 37: The adder Block**

The following are the block parameters as they were used in the set up.

<table>
<thead>
<tr>
<th>ADDER BLOCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icon shape</td>
</tr>
<tr>
<td>List of signs</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

Table 17: Adder Block Parameters

### 3.2.2: THE QPSK DEMODULATOR/CARRIER RECOVERY DESIGN

In many systems, the carrier recovery design is carried out in the demodulator side of the modem. Thus, in considering the demodulator design by implication and extension we do consider the carrier recovery systems.

However, it should be noted that in many BPSK systems the carrier recovery system is separate from the demodulator system due the difference in final expected term. In the carrier recovery system, the final expected term should be a sin term since \( \sin(\varphi - \hat{\varphi}) \) when the difference is small tends to zero. A zero input into the VCO means a phase lock.

Once the system is in phase lock, the output of the demodulator system should be so designed that it is \( \cos(\varphi - \hat{\varphi}) \), where the \( \varphi \) is the phase of incoming BPSK signal and \( \hat{\varphi} \) is the reference phase of the locally generated signal which is in phase lock with the incoming signal. The phase term contains the bit information. For a BPSK the phase is either 0 or 180. Thus, it can be seen that \( \cos 0 \) yields 1 whereas \( \cos 180 \) yields -1.

Thus the cosine term of the phase difference as output to the threshold detector is preferred in demodulation and detection whereas the sine term is ideal for carrier recovery system as there is no steady state errors involved. Nonetheless, in BPSK system it is difficult to realize this in a single system and thus two systems are needed, a carrier recovery and a demodulation and detection. On the other hand, QPSK systems enable both carrier recovery and demodulation and detection within one circuit scheme.
It is in light of this fact that we discuss only the demodulator design as opposed to demodulator and carrier recovery systems design separately.

Below is an illustration of the QPSK re-modulator based carrier recovery system.

![The QPSK re-modulator loop design](image)

**Figure 38: The QPSK re-modulator loop design**

### 3.2.2.1: THE PRODUCT BLOCKS

The Costas based carrier recovery design has four product block (Product, product 1, product 2 and product 3). All four blocks have the same number of inputs and outputs hence all have similar characteristics. These blocks show as well as achieve signal multiplication.

The re-modulator loop carrier recovery design has five block (product 1, product 2, product 3, product 4 and product 5). These also have the same characteristics with one another as well as those used in the Costas based carrier recovery design.

The parameters of all the block are shown below.

<table>
<thead>
<tr>
<th>PRODUCT BLOCK</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs</td>
<td>2</td>
</tr>
<tr>
<td>Multiplication</td>
<td>Element-wise</td>
</tr>
<tr>
<td>Output minimum</td>
<td>[]</td>
</tr>
<tr>
<td>Output maximum</td>
<td>[]</td>
</tr>
<tr>
<td>Output data type</td>
<td>Inherit</td>
</tr>
<tr>
<td>Integer rounding mode</td>
<td>Floor</td>
</tr>
</tbody>
</table>

*Table 18: Product Block Parameters*

### 3.2.2.2: THE ADDERS

Both the Costas based carrier recovery design and the re-modulator loop carrier recovery design have one adder. The adders are similar and they both serve to achieve signal addition.
The parameters of the adder blocks are given below

<table>
<thead>
<tr>
<th>Icon shape</th>
<th>Rectangular</th>
</tr>
</thead>
<tbody>
<tr>
<td>List of signs</td>
<td>++</td>
</tr>
<tr>
<td>Output minimum</td>
<td>[]</td>
</tr>
<tr>
<td>Output maximum</td>
<td>[]</td>
</tr>
<tr>
<td>Output data type</td>
<td>Inherit</td>
</tr>
<tr>
<td>Integer rounding mode</td>
<td>Floor</td>
</tr>
</tbody>
</table>

Table 19: Adder Block Parameters

3.2.2.3: SATURATION BLOCK
The saturation block is used to limit the signal between a given bound due to gain that may be introduced by the filter.

The diagrammatic block representation is given below

![Saturation Block Diagram](image)

Figure 39: A diagrammatic representation of the Saturation block

The block was set with the following parameters.

<table>
<thead>
<tr>
<th>SATURATION BLOCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper limit</td>
</tr>
<tr>
<td>Lower limit</td>
</tr>
<tr>
<td>Output minimum</td>
</tr>
<tr>
<td>Output maximum</td>
</tr>
<tr>
<td>Output data type</td>
</tr>
<tr>
<td>Integer rounding mode</td>
</tr>
</tbody>
</table>

Table 20: Adder Block Parameters

LOW PASS FILTERS
Low pass filters are used to allow only the low frequency components of a signal to pass through their network whereas the high frequency components are attenuated and thus eliminated.

Low pass filters are used to ‘remove’ the double frequency components of the carriers that were a result of mixing that takes place at different stages of the design. Three filters were used in each design and they are identical in their usage.

The filter can be divided into two categories: namely arm filters and lock loop filter. In the Costas based carrier recovery design, low pass filter 1 and low pass filter 1, are the arm filters
whereas low pass filter 2 is the lock loop filter. On the other hand, in the re-modulator loop carrier recovery design, low pass filter 1 and low pass filter 2, are the arm filters whereas low pass filter 3 is the lock loop filter. All the arm filters were designed with common characteristics while both lock loop filters were likewise designed with common characteristics.

In Simulink a low pass filter block was used in this design. It offered robust customization. Below is its diagrammatic representation.

![Low pass filter block diagram](image)

**Figure 40: A diagrammatic representation of a low pass filter**

Given below is the arm low pass filter parameters and characteristics.

<table>
<thead>
<tr>
<th>ARM LOW PASS FILTER</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Impulse response</td>
<td>IIR</td>
</tr>
<tr>
<td>Order mode</td>
<td>Specify</td>
</tr>
<tr>
<td>Order</td>
<td>10</td>
</tr>
<tr>
<td>Frequency units</td>
<td>kHz</td>
</tr>
<tr>
<td>Input sample rate</td>
<td>10</td>
</tr>
<tr>
<td>Pass band frequency</td>
<td>0.075</td>
</tr>
<tr>
<td>Stop band frequency</td>
<td>0.080</td>
</tr>
<tr>
<td>Magnitude constraints</td>
<td>Unconstrained</td>
</tr>
<tr>
<td>Design method</td>
<td>IIR least p-norm</td>
</tr>
<tr>
<td>Structure</td>
<td>Direct form II transposed SOS</td>
</tr>
<tr>
<td>Input processing</td>
<td>Columns as channel</td>
</tr>
</tbody>
</table>

**Table 21: Arm Lowpass Filter Parameters**

The lock loop filter was designed based on control system theory so as to ensure stability of the network as well as achieve a steady state output of approximately 0 volts when frequencies are in synchronism.

Given below is the lock loop filter parameters and characteristics.

<table>
<thead>
<tr>
<th>LOCK LOOP LOW PASS FILTER</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Impulse response</td>
<td>IIR</td>
</tr>
<tr>
<td>Order mode</td>
<td>Specify</td>
</tr>
<tr>
<td>Order</td>
<td>7</td>
</tr>
<tr>
<td>Frequency units</td>
<td>kHz</td>
</tr>
<tr>
<td>Input sample rate</td>
<td>10</td>
</tr>
<tr>
<td>Pass band frequency</td>
<td>0.015</td>
</tr>
<tr>
<td>Stop band frequency</td>
<td>0.025</td>
</tr>
<tr>
<td>Magnitude constraints</td>
<td>Unconstrained</td>
</tr>
<tr>
<td>Design method</td>
<td>IIR least p-norm</td>
</tr>
<tr>
<td>Structure</td>
<td>Direct II form SOS</td>
</tr>
</tbody>
</table>

The lock loop filter was designed based on control system theory so as to ensure stability of the network as well as achieve a steady state output of approximately 0 volts when frequencies are in synchronism.
Given below is the frequency response of the arm filters.

![Figure 41: Filter magnitude and frequency plot](image)

Given below is the lock loop filter frequency response.

![Figure 42: The frequency plot of the Loop filter](image)
3.2.2.5: THE VOLTAGE CONTROLLED OSCILLATOR AND THE 90° PHASE SHIFTER

The Voltage Controlled Oscillator’s output frequency is determined by the value of its input current. It has a quiescent operating frequency. The VCO’s output was phase shifted to yield both a sine and cosine term.

Illustrated below is the design used.

![Diagram of Voltage controlled Oscillator and phase shifter design]

The following were the set parameters of the discrete time VCO.

<table>
<thead>
<tr>
<th>DISCRETE TIME VCO BLOCK PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output amplitude</td>
</tr>
<tr>
<td>Quiescent frequency</td>
</tr>
<tr>
<td>Input sensitivity</td>
</tr>
<tr>
<td>Initial phase</td>
</tr>
<tr>
<td>Sample time</td>
</tr>
</tbody>
</table>

Table 23: Discrete time VCO block Parameters

The phase setting in the second VCO, VCO1, was set to 90° to give a cosine wave output.

3.2.2.6: GAIN AND DELAY BLOCK

The gain blocks were used to add gain into the arm filtered output which was then clipped to give the message signal. This was a result of a failure in the design of the filter to achieve an appropriate gain. Below is the gain block.

![Diagram of Gain block]
The value of gain was set to 100.

The delay block was used to ensure phase match between the transmitted QPSK signal and the re-modulated QPSK signal. Given below is the delay block.

![Figure 45: The Delay block](image)

By scope analysis the value of the delay block that achieved phase synchronism was observed to be 105.

These are all the modules that were used in the project to carry out carrier recovery.
CHAPTER 4: RESULTS AND ANALYSIS

The results were divided into two section for illustrative purposes and thorough follow of the system. These are:

1.) QPSK Modulator system results
2.) QPSK demodulator system results

4.1: QPSK MODULATOR SYSTEM RESULTS
4.1.1: THE DATA SIGNALS

Below is the serial data input at a sample time of 0.025 seconds.

Figure 46: The serial bit stream

Below is the in-phase bit stream as separated from the serial bit stream. It represents the odd bits of the bit stream. The first bit is a redundant bit that is picked at the onset of the flip flop triggering hence should not be considered.

Figure 47: In-phase bit stream
Likewise, in the quadrature data input the first bit is redundant and should be ignored in analysis. This bit stream represents the even data in the serial data stream.

![Figure 48: The quadrature bit stream](image)

The sample time was doubled in the serial to parallel conversion process to 0.05 seconds.

After the serial to parallel conversion the signals were converted to bipolar. Below are the In-phase and Quadrature bit respectively in their bipolar form. They are given below.

![Figure 49: The in-phase bipolar bit stream](image)
4.1.2: THE MODULATED WAVEFORMS

Below is the in-phase modulated waveform, the quadrature modulated waveform and the sum of both respectively. The waveforms are taken in a small range of time because of the frequency value used for the carriers.

Figure 50: The quadrature bipolar bit stream

Figure 51: The in-phase modulated waveform

Figure 52: The quadrature phase modulated waveform
The result of the adding of the two signals is given below.

Figure 53: The transmitted waveform

4.2: QPSK DEMODULATOR SYSTEM RESULTS

The QPSK signal multiplied by the locally generated cosine and sine carrier at a frequency of 120 Hz (for coherent demodulation) yielded the following signals respectively.

Figure 54: QPSK signal and cosine product

Figure 55: The QPSK signal and sine product
The filtered signals are given below. The upper arm filtered signal and the lower arm filtered signal respectively.

![Figure 56: The lower arm filtered signal](image1)

![Figure 57: The upper arm filtered signal](image2)

The filtered signals from the theory are seen to follow the in-phase and the quadrature bit stream respectively. Thus through appropriate amplification the bit streams were obtained as shown below.

![Figure 58: The upper arm/in-phase bit stream](image3)

There is a time delay in the recovered message signals of approximately 0.012 seconds.
4.3: THE REMODULATOR RESULTS

The in-phase bit stream was re-modulated using a cosine carrier while the quadrature bit stream was modulated using the sine wave carrier. The sum of the two waveforms made the QPSK re-modulated signal is given below.
4.4: PHASE TRACKING AND CARRIER RECOVERY RESULTS

After multiplication with the incoming QPSK signal and filtering the error signal into the VCO was observed to be following.

This error signal was seen to vary up and down depending on the delay added by the delay block. At some instances positive at others negative as shown above.
Nevertheless, a steady error constant was continuously observed.

A set at off data was collected by use of a spectrum analyzer at two different quiescent frequencies to determine the behavior of the VCO in analysis.

<table>
<thead>
<tr>
<th>QUISCENT FREQUENCY = 150HZ</th>
<th>CARRIER FREQUENCY (Hz)</th>
<th>VCO FREQUENCY (Hz)</th>
<th>DIFFERENCE (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>156</td>
<td>36</td>
<td></td>
</tr>
<tr>
<td>130</td>
<td>156</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>137</td>
<td>163</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>163</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>163</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>163</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>155</td>
<td>163</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>163</td>
<td>169</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>169</td>
<td>163</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>175</td>
<td>163</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>163</td>
<td>17</td>
<td></td>
</tr>
</tbody>
</table>

Table 24: VCO Frequency characteristic at 150Hz

<table>
<thead>
<tr>
<th>QUISCENT FREQUENCY = 137Hz</th>
<th>CARRIER FREQUENCY (Hz)</th>
<th>VCO FREQUENCY (Hz)</th>
<th>DIFFERENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>137</td>
<td>47</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>143</td>
<td>43</td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>143</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td>120</td>
<td>137</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>130</td>
<td>150</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>137</td>
<td>143</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>137</td>
<td>6</td>
<td></td>
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<tr>
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<td>0</td>
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<tr>
<td>156</td>
<td>163</td>
<td>7</td>
<td></td>
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<tr>
<td>163</td>
<td>150</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>169</td>
<td>137</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>182</td>
<td>137</td>
<td>45</td>
<td></td>
</tr>
</tbody>
</table>

Table 25: VCO Frequency characteristic at 137Hz

From the above data set the VCO was observed not to function as expected. There was no tracking of the carrier. The input error phase term is seen to have assumed a non-linear relationship to the error phase error term of the incoming QPSK signal and the re-modulated QPSK signal.
CHAPTER 5: DISCUSSIONS AND CONCLUSIONS

Much of the project was carried out successfully with the main aims of the project being achieved save for the demonstration of carrier recovery which was not achieved due to an inefficient design in the phase lock loop filter.

The cause for this, through research, was seen to might have be the use of an IIR filter in the PLL loop filter. IIR filter were seen not to offer a linear phase relationship. This non-linearity is thought to be the cause of the results obtained.

Regrettably, a correction was not made in the design to factor in this aspect due to limited time constraints.

In general, the project was to be carried out in three steps: modulation, demodulation and carrier recovery.

In modulation, serial to parallel conversion of the bit stream was well illustrated resulting in a set of odd bits and even bits which were later modulated simultaneously with carriers at quadrature. A change from a unipolar to a bipolar signal was also shown and finally modulation carried out after which the two quadrature signal were added to give the QPSK signal. This was the transmitted signal.

In demodulation, initially the VCO was hard set to lock on the carrier frequency to demonstrate coherent demodulation. The incoming QPSK signal was multiplied by both a sine and a cosine carrier of the same frequency and the resulting signal filtered. Here an IIR filter was used and seen to function correctly. The resulting signal was seen to give the difference in phase as a function of amplitude. To this amplitude a gain was added and and the original message signal was seen to be obtained.

Through the demodulated data the re-modulation process was carried out effectively with little disparity between the signals in the modulator side and the re-modulator signals save for a delay that was introduced in reconstruction of the message signal. Carrier tracking was not achieved as explained earlier. This is one of the major regrets of this project.
CHAPTER 6: RECOMMENDATION

During the undertaking of the project it was noted that many of the Simulink blocks used were blocks that represented certain circuit configurations that was just lumped into one block. This does not give a good insight into the electronics involved in the circuitry themselves and would hinder a hardware implementation of the same. It is therefore recommended that in the design much of the design be in electrical component format in the blocks as opposed to lumped blocks that do not clearly show the circuits within.

However, this would require an additional time in the length of the undertaking of the project.
CHAPTER 7: REFERENCES


