UNIVERSITY OF NAIROBI

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND INFORMATION ENGINEERING

A CLOCK LOCKED TO 50HZ AC LINE

PROJECT INDEX: PRJ 40

BY

OGECHI JOY NANCY

F17/29777/2009

SUPERVISOR: DR. DHARMADHIKARY

EXAMINER: DR. W. MWEMA

A project report submitted in partial fulfillment of the Requirement for the award of the degree Of Bachelor of Science in ELECTRICAL AND INFORMATION ENGINEERING of the University of Nairobi 2014

Submitted on: Monday 28th April, 2014

DECLARATION OF ORIGINALITY

FACULTY/ SCHOOL/ INSTITUTE: Engineering

DEPARTMENT: Electrical and Information Engineering

COURSE NAME: Bachelor of Science in Electrical & Information Engineering

NAME OF STUDENT: OGECHI JOY NANCY

REGISTRATION NUMBER: F17/29777/2009

COLLEGE: Architecture and Engineering

WORK: A CLOCK LOCKED TO 50HZ AC LINE

1) I understand what plagiarism is and I am aware of the university policy in this regard.
2) I declare that this final year project report is my original work and has not been submitted elsewhere for examination, award of a degree or publication. Where other people's work or my own work has been used, this has properly been acknowledged and referenced in accordance with the University of Nairobi's requirements.
3) I have not sought or used the services of any professional agencies to produce this work.
4) I have not allowed, and shall not allow anyone to copy my work with the intention of passing it off as his/her own work.
5) I understand that any false claim in respect of this work shall result in disciplinary action, in accordance with University anti-plagiarism policy.

Signature:

……

Date:

……

DEDICATION

I dedicate this project to all those who have stood by me in every step of the way, assisted me in every way they could and made sure I never lacked the zeal and belief that I needed to make my project a success.

These people include: - **my parents** for the moral and financial support they have offered me, and **my siblings** for the guidance and inspiration they have given me throughout my journey of education.

ACKNOWLEDGEMENT

First and foremost, I am grateful to the Almighty God for His unconditional love, peace, strength and abundant protection throughout the course of my project.

Secondly, I acknowledge the enormous input by my supervisor, Dr. Dharmadhikary for the useful comments and suggestions which have led to the improvement of this project and for the guidance and moral support that he granted unto me during the development of this project.

I would also like to acknowledge my entire family and friends for the all round support they offered me during the course of my studies.

Lastly I would like to thank my colleagues for their encouragement, support and advice on various improvements that seemed necessary on the project. I specifically take this opportunity to thank my classmates Kenneth Mugo, Kennedy Njoroge, Dennis Onyango and Michelle Ngure for their time and input during the journey of making this project a success.

TABLE OF CONTENTS

LIST OF FIGURES

Figure 4.2 (b) Output waveform of VCO of input 50Hz, resistance 253.6 ohms

Figure 4.2 (c) Output waveform of VCO of input 50Hz, resistance 4.52 kilohms

Figure 4.2 (d) Output waveform of VCO of input 50Hz, resistance 4.52 kilohms

LIST OF TABLES

LIST OF ACRONYMS

PLL	Phase-locked Loop
APLL	Analogue Phase-locked Loop
ADPLL	All Digital Phase-locked Loop
DPLL	Digital Phase-locked loop
VCO	Voltage Controlled Oscillator
PD	Phase Detector
PC	Phase Comparator
LF	Loop filter
XOR	Exclusive OR
JK (flip flop)	Jack Kilby flip flop
D (flip flop)	Dangling flip flop
TTL	Transistor Transistor logic
CMOS	Complementary Metal Oxide semiconductor
ECL	Emitter Coupled Logic
DCO	Digital Controlled Oscillator
NCO	Numerically Controlled Oscillator
SPPL	Software Phase locked loop
DSP	Digital signal processor
PFD	Phase Frequency Detector
AC	Alternating Current
DC	Direct Current
PCB	Printed Circuit Board
DN	DOWN

ABSTRACT

This project aims at designing a circuit that can generate a clock locked to 50Hz mains using the technique of a phase-locked-loop multiplier.

Prior to design, a revision of Phase Locked Loop (PLL) theory was performed to give the author a firm starting point of how a PLL works, the available types and their availability in the market.

The PLL is a closed loop frequency system that locks the phase of an output signal to an input reference signal. It operates by trying to lock to the phase of an accurate input signal through the use of its negative feedback path.

The design flow process included design and simulation of the system. The application chosen in designing the PLL was frequency multiplication and this was carried out using a modulo-n counter locked to the feedback path thus generating a multiple of the input reference frequency.

CHAPTER ONE: INTRODUCTION

1.1 Background

The Phase-Locked-Loop (PLL) is highly desirable in almost every communication system. It is a very useful and versatile building block for many subsystems used in the implementation of modern communication systems. It works as an electronic feedback system; this way a small disturbance in the system manipulates the feedback input to the system to minimize this error. As it name suggests, the phase locked loop operates by trying to lock to the phase of a very accurate input signal through the use of its negative feedback path. It is suitable for a wide variety of applications such as: tone decoding, AM radio receivers, frequency demodulators, frequency multipliers, frequency dividers, carrier and symbol synchronizer and as frequency synthesizers.

There has traditionally been some reluctance to use PLLs, partly because of the complexity of discrete PLL circuits and partly because of a feeling that they could not be counted on to work reliably. The phase locked loop was first described in early 1930s, where its application was in the synchronization of the horizontal and vertical scans of television. Later on with the development of integrated circuits, the first barrier to their acceptance vanished and it found uses in many other applications. The first PLL ICs came in existence around 1965, and were built using purely analog devices. Recent advances in integrated circuit design techniques have led to an increased use of the PLL as it has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

1.2 Problem Statement

PLL has a wide range of applications. Most of the frequency multiplication applications employ a phase locked loop circuit as this technique offers many advantages such as minimum complex architecture, low power consumption and a maximum use of Large Scale Integration technology. The problem thus posed is to implement a system to be used to generate a clock locked to mains using the PLL multiplier technique.

1.3 Main Objectives

The main objective of this project is to design a system using a PLL multiplier that will generate a clock locked to mains. This system will thus output a frequency that is a multiple of the input frequency, which in our case is the 50Hz mains.

1.4 Project Scope

The project entails designing a circuit using the PLL technique that can generate an output clock that is a multiple of 50Hz mains input and have this output synchronize with the 50Hz input so as to reach a lock state.

CHAPTER TWO: LITERATURE REVIEW

2.1 Introduction

The phase locked loop is a very useful and versatile building block in the frequency domain. It is a type of an electronic closed loop feedback system which is used to synchronize the output signal of an oscillator with a reference signal in both frequency and phase. While synchronized in frequency, the phase difference between the output signal and input signal is zero, or very small. It works in much the same way as a general feedback loop which acts in most control systems, e.g. electronic, mechanical as shown in figure 2.1. If the output is different from the desired value; the mixer produces an error signal which is then amplified and corrects the output.

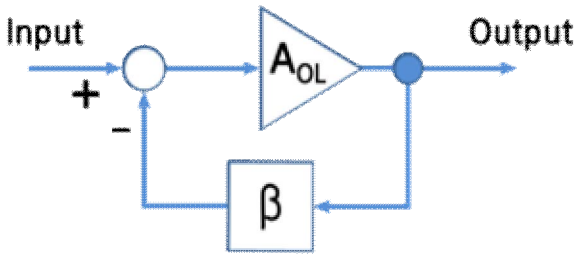


Figure: 2.1. A general feedback loop

A basic PLL consists of three fundamental blocks including;

- A phase detector/ phase comparator
- A low-pass filter
- A voltage controlled oscillator; in an arrangement shown below.

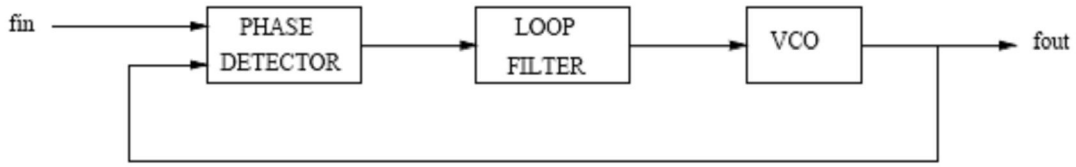


Figure: 2.2. Components of phase-locked loops

The phase detector compares the phase of the output signal, f_{vco} to the phase of the reference signal, f_{in}. If there is a phase difference between the two signals, it generates an output voltage which is proportional to the phase error of the two signals. This output voltage passes through the loop filter and then as an input to the voltage controlled oscillator (VCO) controls the output frequency, f_{out}. Due to this self correcting technique the output signal will be in phase with the reference signal. When both signals are synchronized the PLL is said to be in lock condition. The phase error between the two signals is zero or almost zero at this point.

As long as the initial difference between the input signal and the VCO is not too big the PLL eventually locks onto the input signal. This period of frequency acquisition is referred to as pull-in time this can be very long or very short depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the phase detector. PD, voltage controlled oscillator and on the low pass filter.

2.2 Types of Phase-Locked Loops

Generally speaking, the monolithic PLLs can be classified into two groups:-

- **Analog or Linear PLL (APLL)**
- **Digital PLL (DPLL)**

While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

2.2.1 Analog or Linear PLL (APLL)

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals.

Since this mixing is true analog multiplication, the phase comparator's output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty

cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications. The loop filter may be passive or active and results in the loop being either first-order or second-order.

2.2.2 Digital PLL (DPLL)

The Digital PLL is like the analog PLL but with a digital phase detector (such as XOR, edge-trigger JK, phase frequency detector). It may have a digital divider in the loop. For the digital PLLs that employ a two-input Exclusive-OR gate as the phase detector, when the digital loop is locked to f_{out}, there is an inherent phase error of 90 that is represented by asymmetry in the output waveform. Also, the phase detector's output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase detectors achieve locking by synchronizing the "edges" of the input and VCO frequency wave shapes. The phase detector produces an error voltage that is proportional to the time difference between the edges; i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the XOR approach. However, time line, on the input and VCO frequencies is translated into phase error line that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle; This is a key consideration in PLL applications utilizing counters where wave shapes usually aren't symmetrical; i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("l" to "O") transition of the waveform. CMOS, 12L, and ECL are better suited for leading edge triggering ("O" to "1").

2.2.3 All Digital PLL (ADPLL)

In all digital PLL, all the components and signals are digital. The VCO is replaced by a digitally controlled oscillator (DCO) which is also called a numerically controlled oscillator (NCO).

2.2.4 Software PLL (SPLL)

The software PLL is implemented by a hardware platform such as a microcontroller or a digital signal processor (DSP). The phase locked loop is realized by software. This allows for flexibility because a large number of different algorithms can be developed. The analysis of the loop filter is done using the z-transform.

2.3 Components of Phase-Locked loop

2.3.1 Phase Detector / Phase Comparator

A phase detector or phase comparator is a frequency mixer, analog multiplier or logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs. Phase detectors for PLL circuits may be classified in two types.

1) A Type I detector designed to be driven by analog signals or square-wave digital signals and produces an output pulse at the difference frequency. The Type I detector always produces an output waveform, which must be filtered to control the PLL VCO.
2) A type II detector is sensitive only to the relative timing of the edges of the input and reference pulses, and produces a constant output proportional to phase difference when both signals are at the same frequency. This output will tend not to produce ripple in the control voltage of the VCO.

2.3.1.1 XOR Gate Phase Detector

This is the most basic type of phase detector. It produces error pulses on both falling and rising edges. Figures 2.3 (a)-(d) give a detailed analysis of the XOR PD when the reference (Φ_{ref}) and feedback signals (Φ_{vco}) are out of phase by zero, $\Pi/2$, and Π respectively.

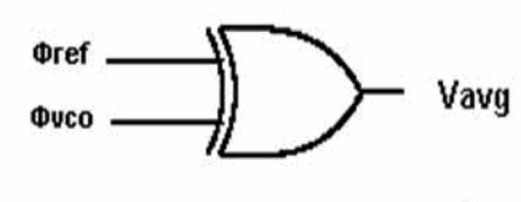


Figure 2.3 (a) XOR phase Detector

Table 1: XOR GATE TRUTH TABLE

XOR Gate states		
Øref	**Øvco**	**Vavg**
0	0	0
0	1	1
1	0	1
1	1	0

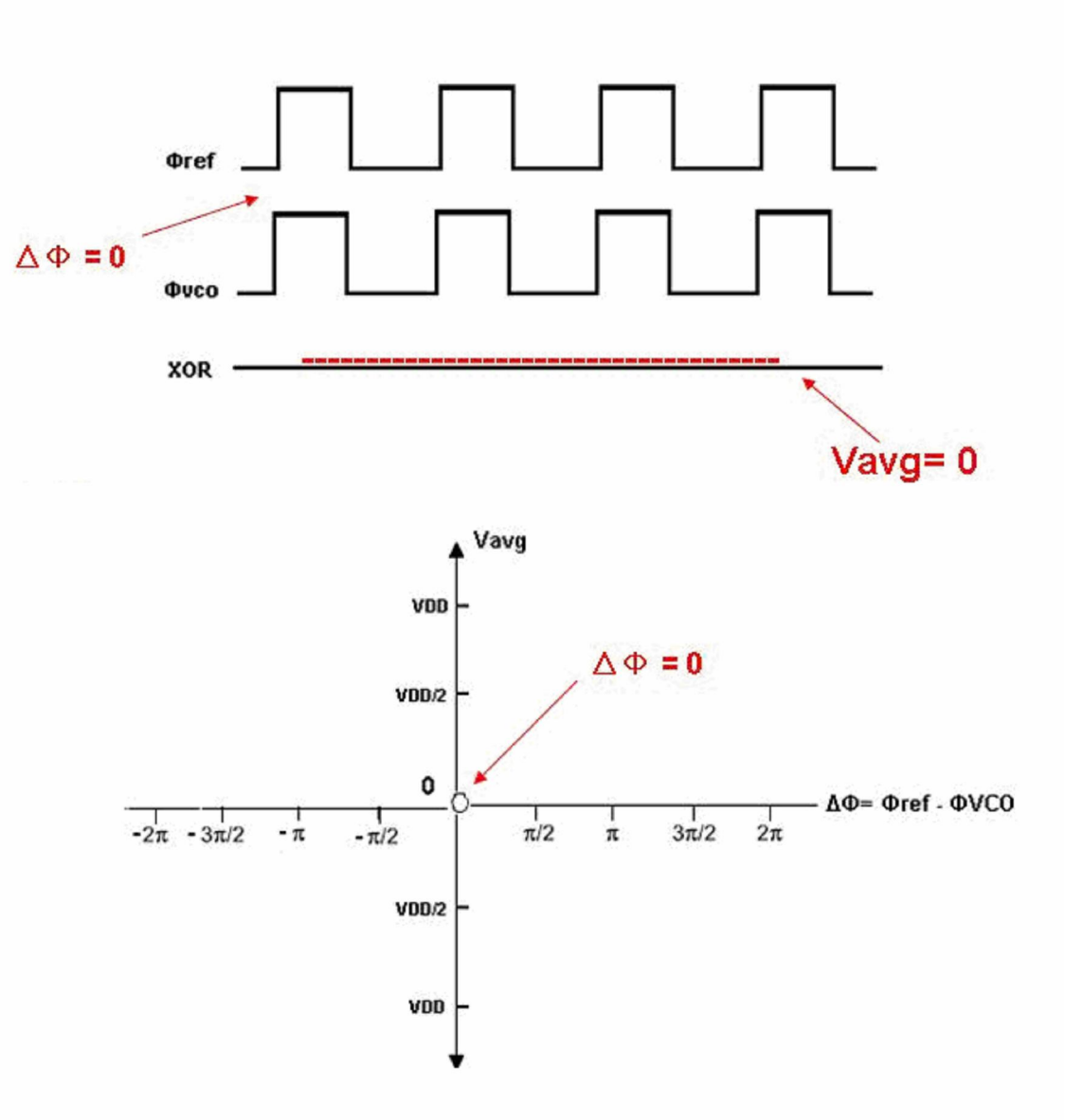


Figure 2.3 (b) Phase Difference= zero

In Figure 2.3 (b) above, the phase difference between the two signals is zero also referred to as a locked phase. The average output, V_{avg}, from the XOR gate is zero for this case. The XOR input/output characteristic graph is a plot of V_{avg} versus the phase difference.

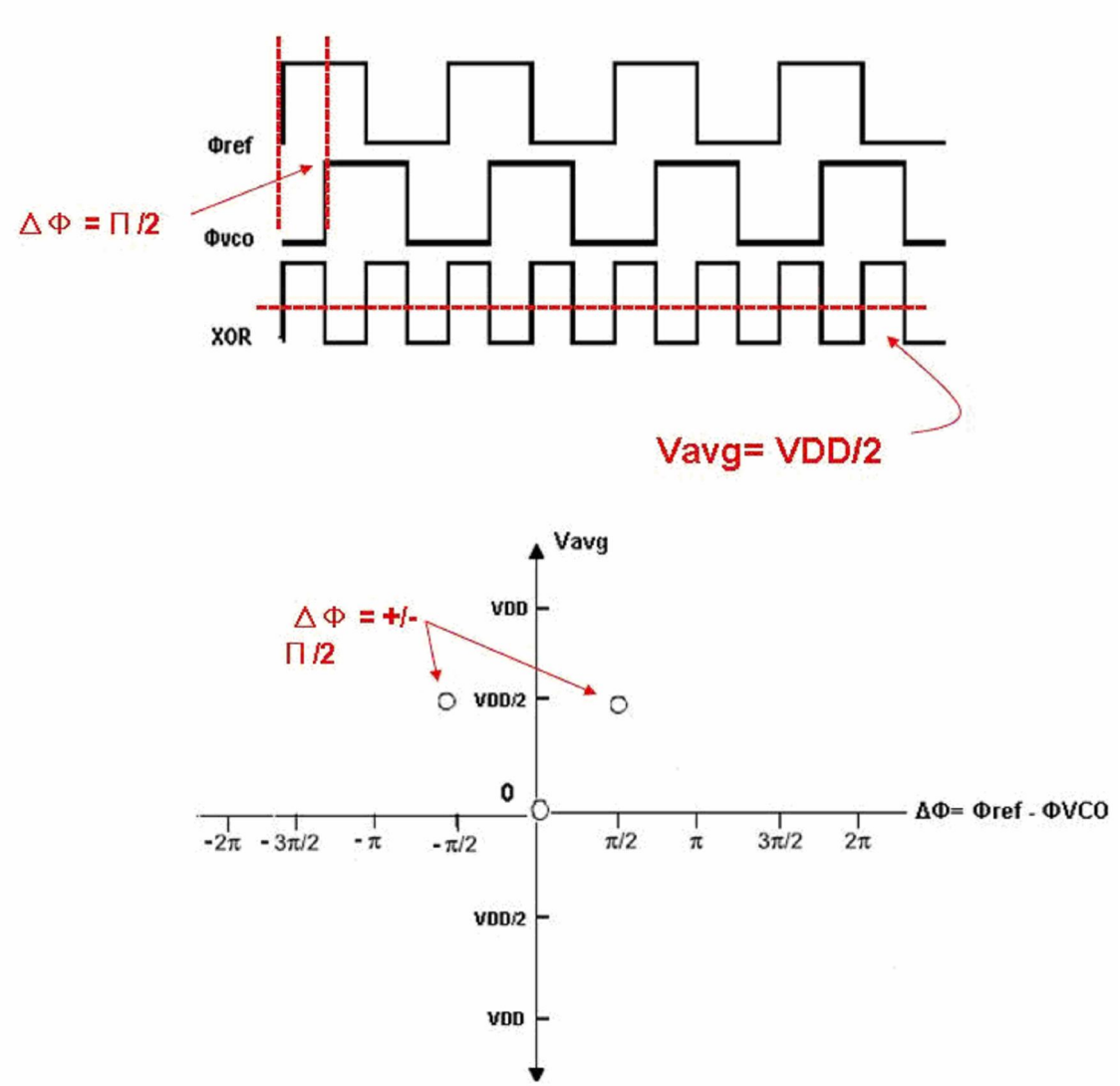


Figure 2.3 (c) Phase Difference = Π/2

In Figure 2.3 (c) above, the phase difference between the two signals is Π/2.The average output, V_{avg}, from the XOR gate is $V_{DD} / 2$ for this case.

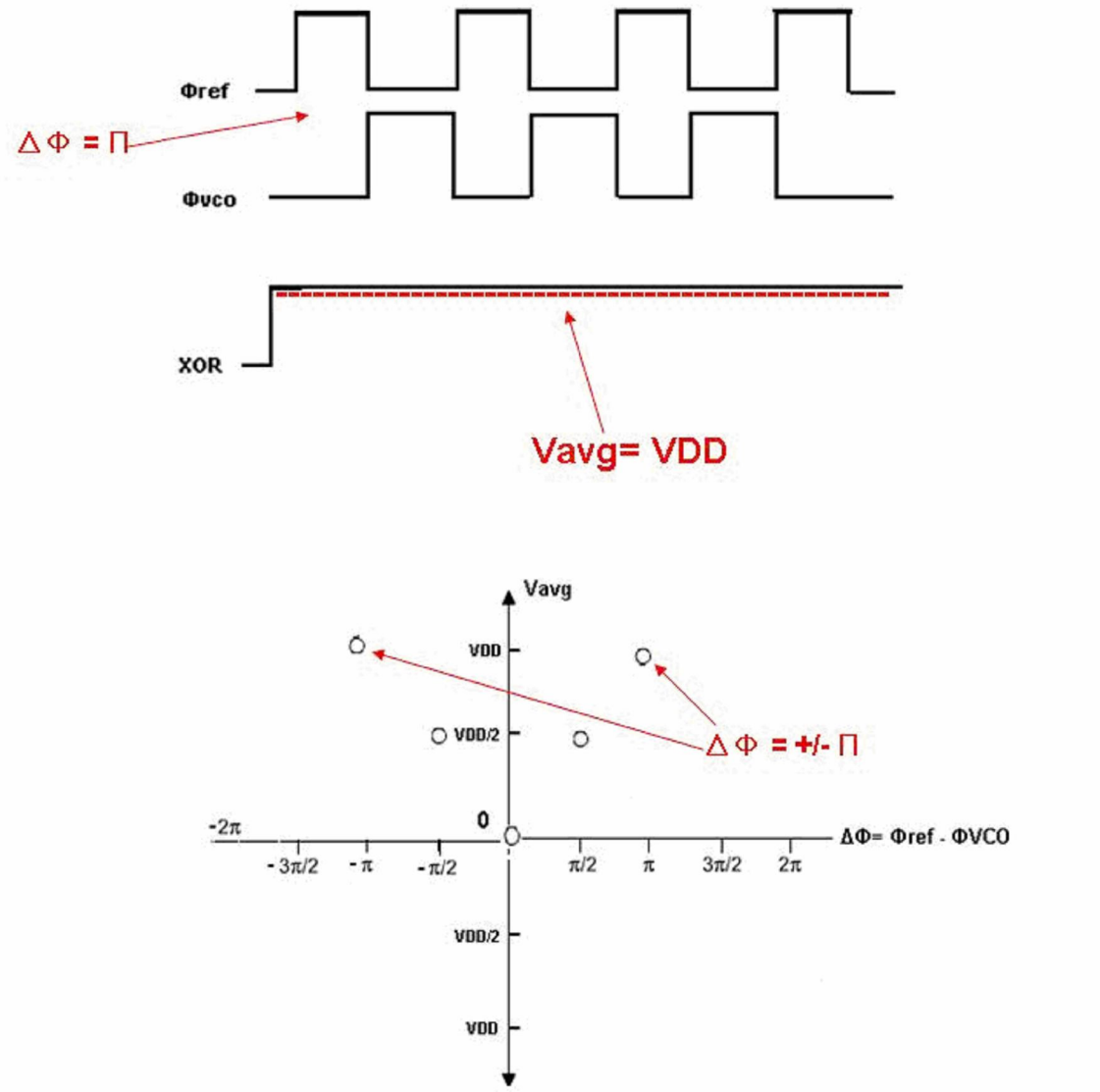


Figure 2.3 (d) Phase Difference = Π

In Figure 2.3(d) above, the phase difference between the two signals is Π. The average output, V_{avg}, from the XOR gate is V_{DD} for this case.

From figures 2.3(c) and (d), the accumulation of points from the phase differences zero, Π/2, and Π are plotted. The final graph is shown in figure 2.3(e). This is the XOR PD characteristic plot. This plot enables us to observe the PD output for a range of phase differences.

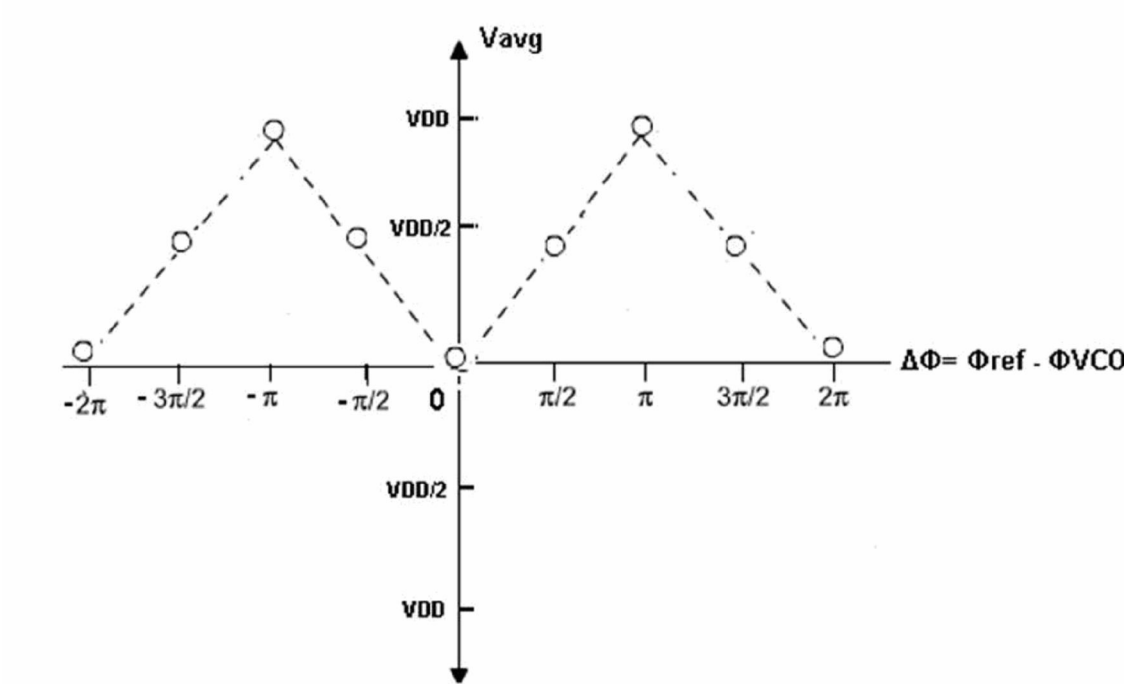


Figure 2.3 (e) PD Characteristic graph of phase differences ranging from 0 to 2Π

The major disadvantage of XOR PD is that it can lock onto harmonics of the reference signal and most importantly it cannot detect a difference in frequency.

2.3.1.2 Phase Frequency Detector

These circuits have the advantage that while the phase difference is between -180 degrees to + 180 degrees, a voltage proportional to the phase difference is given. Beyond this the circuit limits at one of the extremes. In this way no AC component is produced when the loop is out of lock and the output from the PD can pass through the filter to bring the PLL into lock. Another advantage is that it can detect a difference in phase and frequency between the reference and feedback signals. Unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking harmonics.
The block diagram of a PFD is shown below:

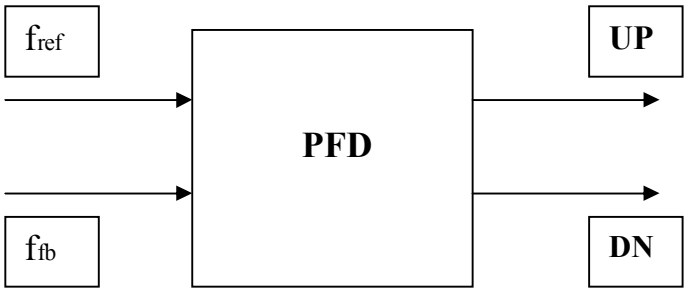


Figure 2.4 Phase Frequency Detector block diagram

The Phase Frequency Detectors are of two types:

• ***Edge triggered JK flip flop phase frequency detector:*** This form of phase comparator is used in some designs.

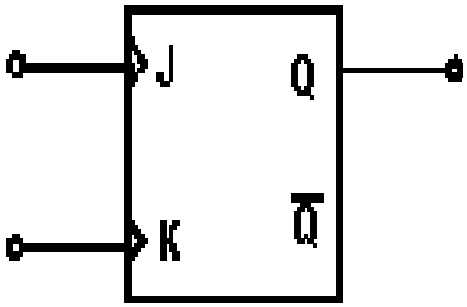


Figure 2.5(a) JK Flip Flop

The idea behind the JK flip flop based comparator is that it is a sequentially based circuit and this can be used to provide two signals: one to charge, and one to discharge a capacitor.

Often when using this form of phase detector, an active charge pump is recommended.

Table 2: JK Flip Flop States table

JK Flip Flop States		
input1	**input2**	**Qn+1**
0	0	Qn
0	1	0
1	0	1
1	1	Qn bar

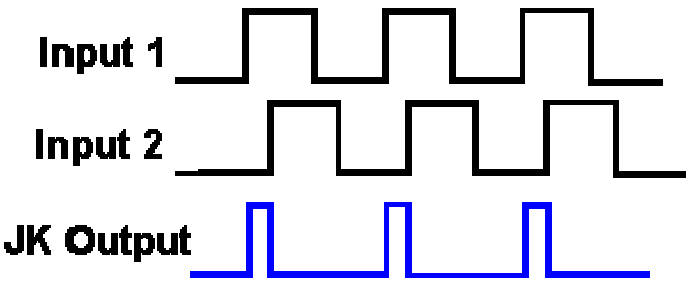


Figure 2.5(b) JK Flip Flop phase detector waveforms

These waveforms can be interpreted and it is found that the overall response appears as below.

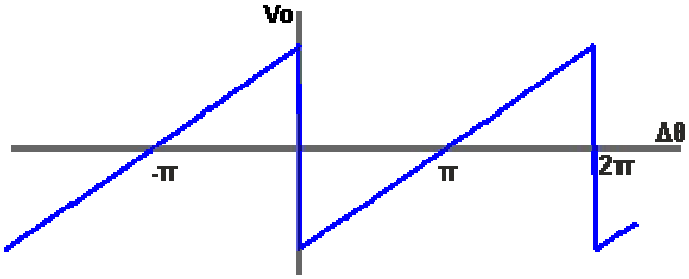


Figure 2.5(c) JK flip flop phase detector response

• ***Dual D type phase comparator:*** This type of phase frequency detector uses two D type flip flops and an NAND gate, although there are a number of slightly different variants. This type of phase comparator is possibly the most widely used form of detector because of its performance and ease of design and use.

The circuit for the dual D-type comparator uses the two D-type flip flops with the reference and VCO signals being compared entering the clock inputs, one on each D-type. The D inputs are connected to VDD- always remaining high. The outputs are either 'UP' or 'DN' pulses. The NAND gate output is fed to the reset, R, inputs of both D-types. The inputs to the NAND gate are taken from the Q outputs and the output to the loop filter being taken from one of the Q outputs.

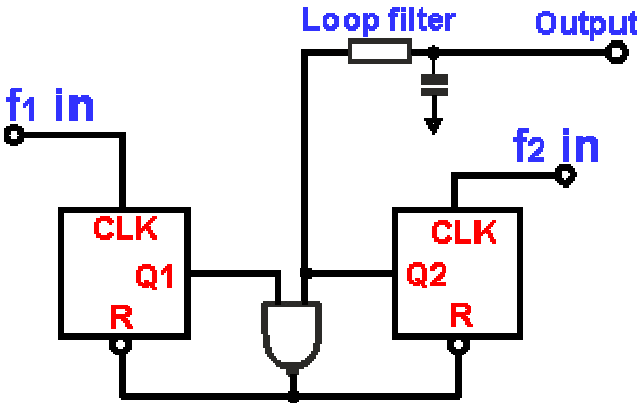


Figure 2.6 (a) Dual D-Type phase detector circuit

The PFD circuit above in Figure 2.6(a) can be analyzed in two different ways—one way in which f_1, the reference frequency, leads f_2, the feedback frequency and the other in which f_2 leads f_1. The term "lead" in this case means that the signal is faster or in the lead of the other.

The first scenario is as shown in Figure 2.6(b)

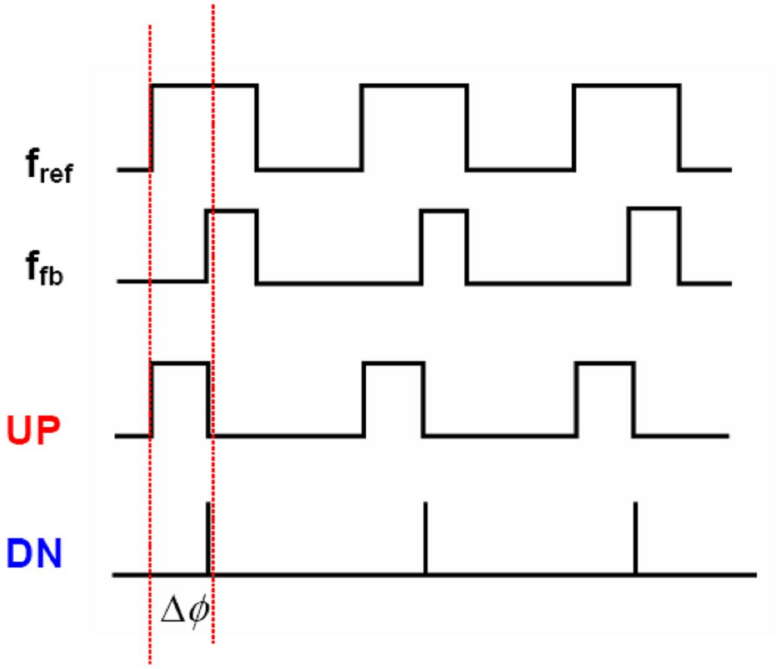


Figure 2.6 (b) f_{ref} leads f_{fb}

When f_{ref} leads f_{fb}, an UP pulse is generated. The UP pulse is the difference between the phases of the two clock signals. This UP pulse indicates to the rest of the circuit that the feedback signal needs to speed up or "catch up" with the reference signal. Ideally, the two signals should be at the same speed or phase.

The other scenario is when feedback signals leads the reference signal as shown in Figure 2.6(c).

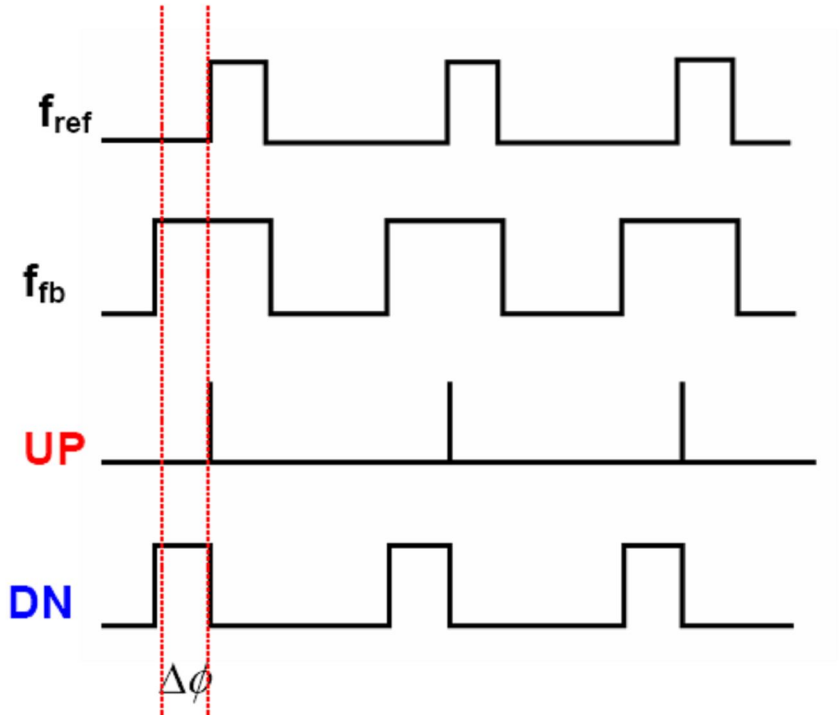


Figure 2.6 (c) f_{ref} lags f_{fb}

The feedback signal leads the reference signal, which generates a DN signal. This DN signal indicates to the rest of the circuit that the feedback signal is faster than the reference signal and needs to slow down.

2.3.2 Low Pass loop Filter

The function of the loop filter is to take the digital up and down error pulses from the phase detector and convert them into an analog control voltage to be fed into the VCO. The output of the PD consists of a DC component superimposed with an AC component. The AC part is undesired as an input to the VCO; hence a low pass filter is used to remove high frequency AC component and noise from the output of the phase detector. The loop filter affects the dynamic characteristics of the PLL including bandwidth, capture and lock ranges and transient response.

If the filter has a very low cut-off frequency, then the changes in tune voltage will only take place slowly, and the VCO will not be able to change its frequency as fast because a

filter with a low cut-off frequency will only let low frequencies through and these correspond to slow changes in voltage level.

On the other hand, a filter with a higher cut-off frequency will enable the changes to happen faster. However when using filters with high cut-off frequencies, care must be taken to ensure that unwanted frequencies are not passed along the tune line with the result that a spurious signal is generated.

The loop filter also governs the stability of the loop. If the filter is not designed correctly then oscillations can build up around the loop, and large signals will appear on the tune line. This will result in the VCO being forced to sweep over wide bands of frequencies. The proper design of the filter will ensure that this cannot happen under any circumstances. A simple LP is as shown in the figure below.

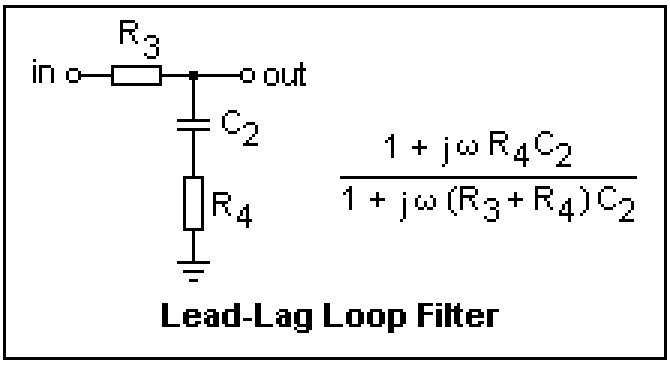


Figure 2.7 Low pass loop filter

2.3.3 Voltage Controlled Oscillator (VCO)

The voltage-controlled oscillator varies the output frequency proportional to input voltage from the loop filter. The DC level output of a low-pass filter is applied as control signal to the voltage-controlled oscillator (VCO). The output frequency of the VCO is directly proportional to the input DC level. The VCO frequency is adjusted till it becomes equal to the frequency of the reference input signal. During this adjustment, PLL goes through three stages-free running, capture lock and phase lock. Best operation is obtained if the centre frequency of the VCO is set with the DC bias voltage midway in its linear

operating range. The amplifier allows this adjustment in DC voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the PD are of the same frequency although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed DC voltage to the VCO. Variation in the input signal frequency then causes variation in the DC voltage to the VCO. Within a capture-and-lock frequency range, the DC voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the PD contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower-frequency component of the signal so that the loop can obtain lock between input and VCO signals.

Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the range of frequencies centered about the VCO free-running frequency f_r, over which the output signal frequency of the VCO can acquire lock with the input signal frequency. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the lock range.

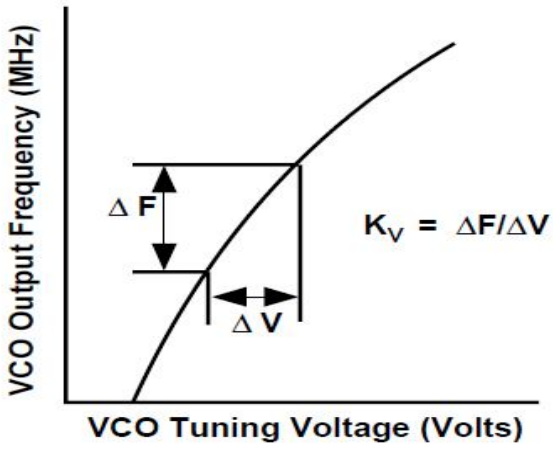


Figure 2.8 VCO characteristics

Where $K_v = VCOgain\ \left(\frac{\frac{rad}{V}}{sec}\right)$

2.4 Terminologies associated with phase locked loop

2.4.1 Locked state

This is a condition in which the frequency and phase of the generated signal is equal to the frequency and phase of the reference signal.

2.4.2 Free running frequency

This is the free oscillating frequency of the VCO when it is in an unlocked state.

2.4.3 Lock range (Hold-in range)

When the PLL is in the phase-locked state, the frequency range in which the frequency of the input reference signal, can slowly be pulled away from the free running frequency of the VCO but still maintain the phase-locked condition is called the hold-in range or lock range. The lock range is much larger than the capture range.

2.4.4 Capture range(Lock-in range)

When the PLL is not in the phase-locked state, if the frequency of the input signal, slowly approaches the free running frequency of the VCO, the frequency range in which the input signal becomes phase-locked is called the lock-in range or capture range.

2.4.5 Acquisition time (Lock-up time)

The amount of time required for the loop to phase lock is called lock-up time or acquisition time.

2.5 Some Phase Locked Loop Applications

2.5.1 DC Motor speed control

Many electro-mechanical systems, such as magnetic tape drives, require precise speed control, particularly during start and stop operations. This can be achieved by incorporation the motor within a phase-locked loop. When the motor rotates, the tachogenerator produces an AC signal whose frequency is proportional to the speed of

the motor. The signal is then fed to the phase detector together with the control signal. The phase-locked loop detects any difference between the two phases and drives the motor so that there is a cycle-for-cycle correlation between the control frequency and speed of the motor.

2.5.2 Clock recovery

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator. Typically, some sort of redundant encoding is used, such as 8b/10b encoding.

2.6 Frequency Multiplication

One of the most common uses of a PLL is in frequency multiplication. A frequency multiplier generates an output frequency that is a multiple of a stable reference frequency. Frequency multiplication is commonly done in RF/Microwave equipment to generate high stability, low noise signals.

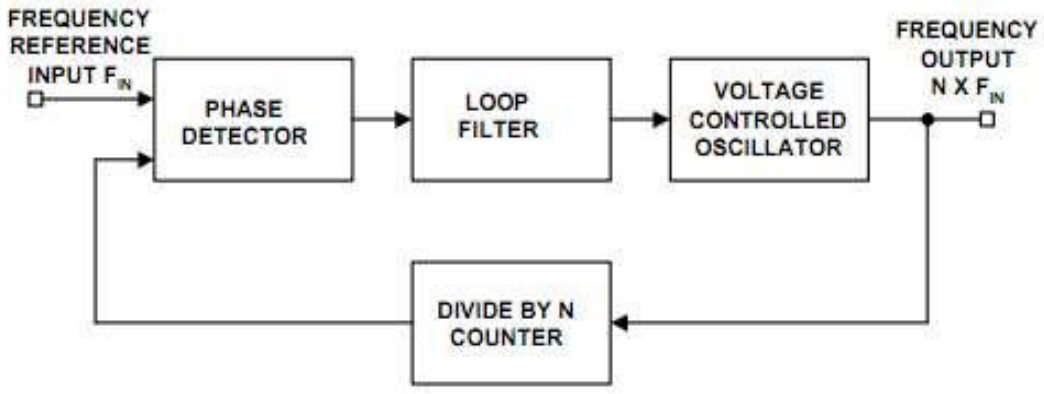


Figure 2.9 Block diagram of a frequency multiplier

In the above block diagram, a frequency divider is inserted between the output of the VCO and the phase detector so that the loop signal to the PD is at frequency: f_{OUT} while the output of the VCO is N f_{OUT}. This output is a multiple of the input frequency as long

as the loop is in lock. The desired amount of multiplication can be obtained by selecting a proper divide-by N network where N is an integer.
The relationships are thus expressed as below:

$$N f_{IN} = N f_{OUT}$$
$$N f_{IN} / N = N f_{OUT} / N$$

CHAPTER THREE: DESIGN AND IMPLEMENTATION OF THE PHASE LOCKED LOOP MULTIPLIER CIRCUIT

3.1 Introduction

This chapter seeks to explain in depth the process used in the implementation and operation of the PLL multiplier. The design entailed the following:

i. Software simulation

ii. Hardware implementation

iii. Printed Circuit Board

The project design can be summarized in form of a block diagram as shown in fig 3.1 below:

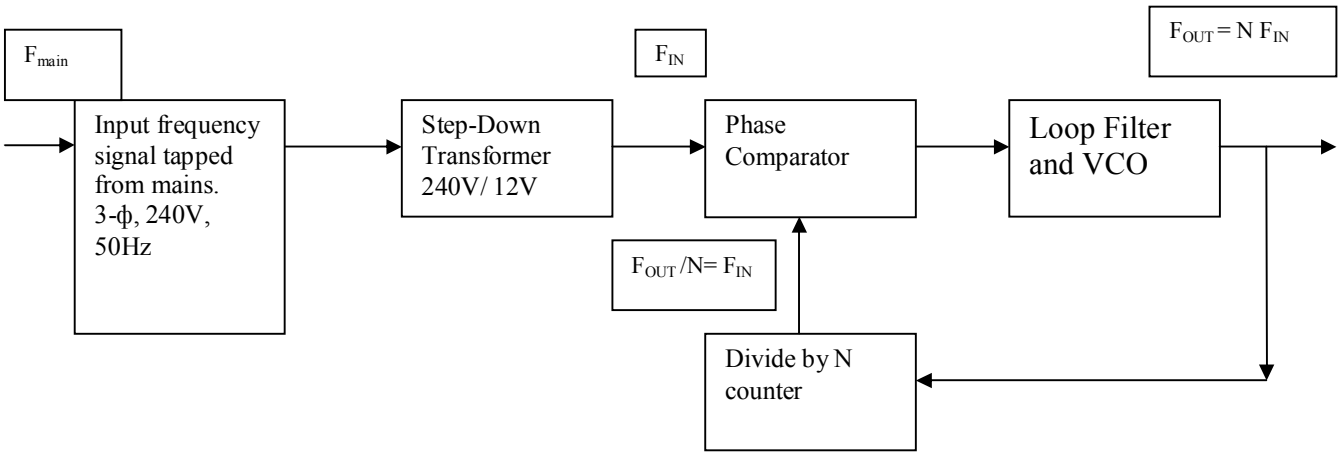


Figure 3.1 Block diagram of the overview of project design

The flow chart shown in fig 3.2 depicts the sequence of events used in the implementation of the project.

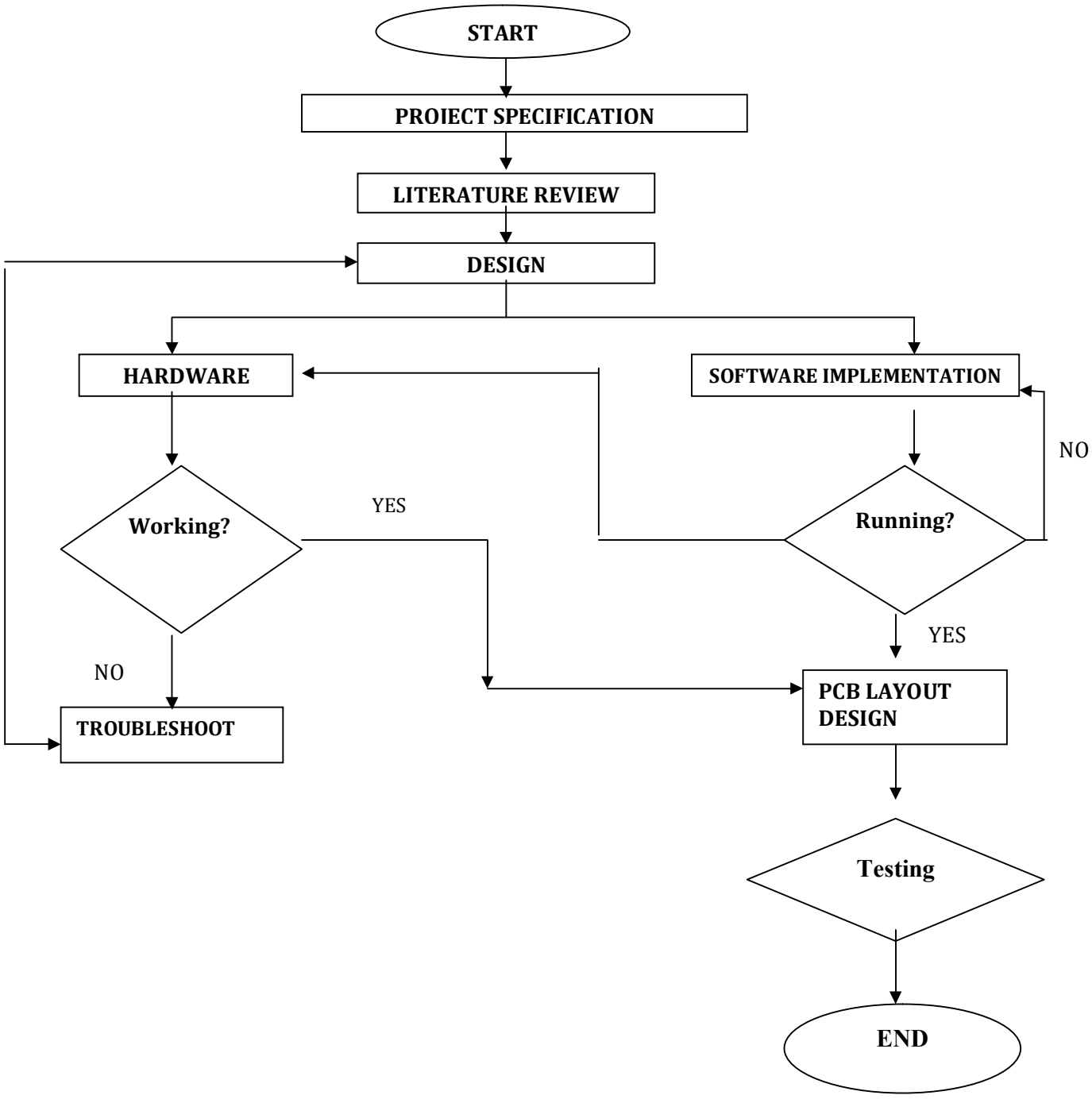


Figure 3.2 Project implementation flow chart

3.2 PLL Design Calculations

The frequency chosen to be generated was 200,000Hz. A standard PLL scheme was chosen with a divide by n counter added between the VCO and the phase detector.

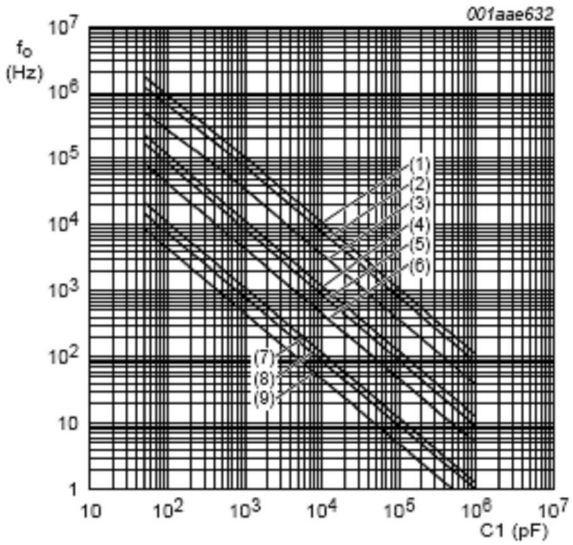
Minimum frequency= 20Kilohertz

The VCO was varied using resistors R1, R2 and C1. These values were chosen using the design graph on the 4046 datasheet.
The recommended range of R3 and R4 is 10kilo ohm to 1 mega ohm. For C1 it is 50 picofarad to any practical value. Using the graph below we thus determined R3 and R4 as 200 K and 10 K respectively.

The loop filter values were calculated as:

$$cut\ off\ frequency\ = \frac{1}{2\pi RC}$$

where R = 4.3 Mega ohms and
C= 1 microfarad



T_{amb} = 25 °C; VCO_IN at $0.5V_{DD}$; INH_IN at V_{SS}; R2 = ∞.

Lines (1), (4), and (7): V_{DD} = 15 V;

Lines (2), (5), and (8): V_{DD} = 10 V;

Lines (3), (6), and (9): V_{DD} = 5 V;

Lines (1), (2), and (3): R1 = 10 kΩ;

Lines (4), (5), and (6): R1 = 100 kΩ;

Lines (7), (8), and (9): R1 = 1 MΩ.

Fig 7. Typical center frequency as a function of capacitor C1

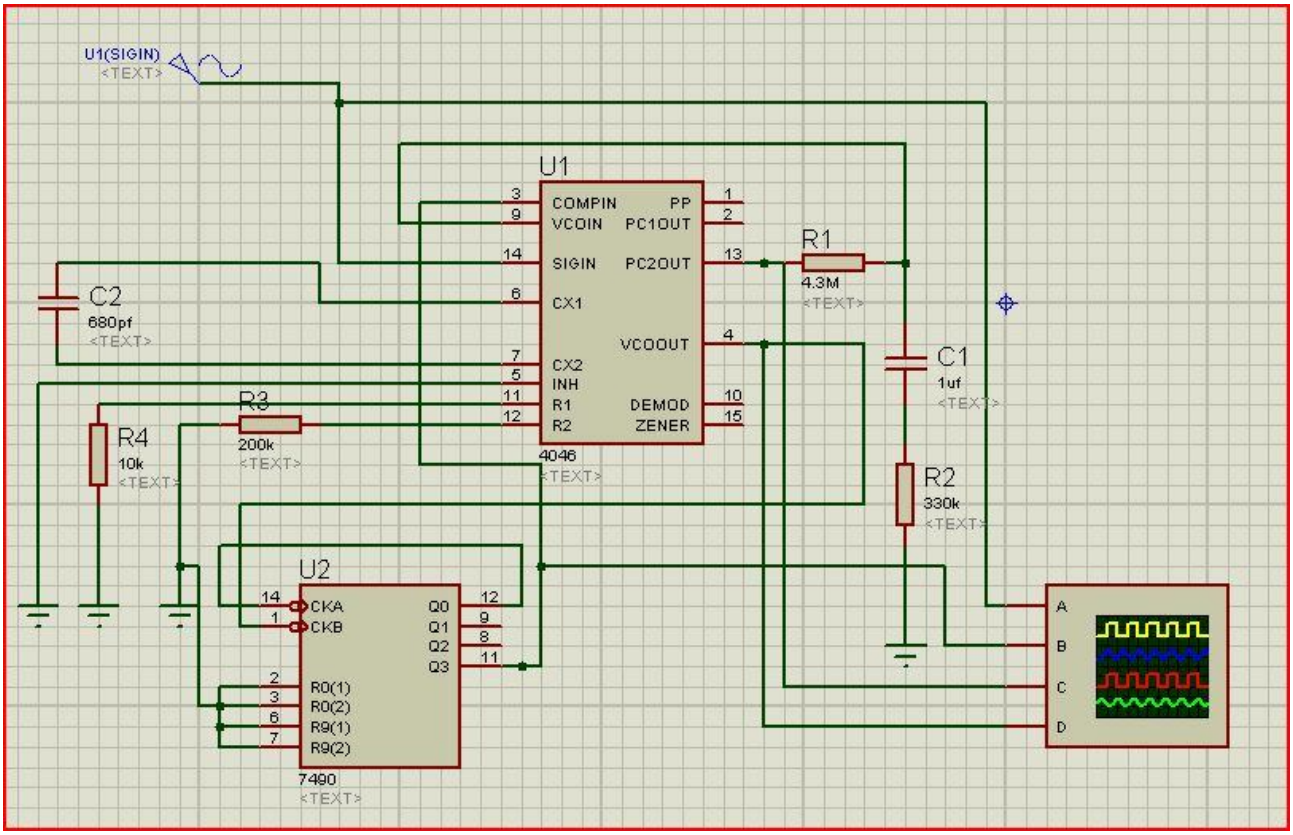
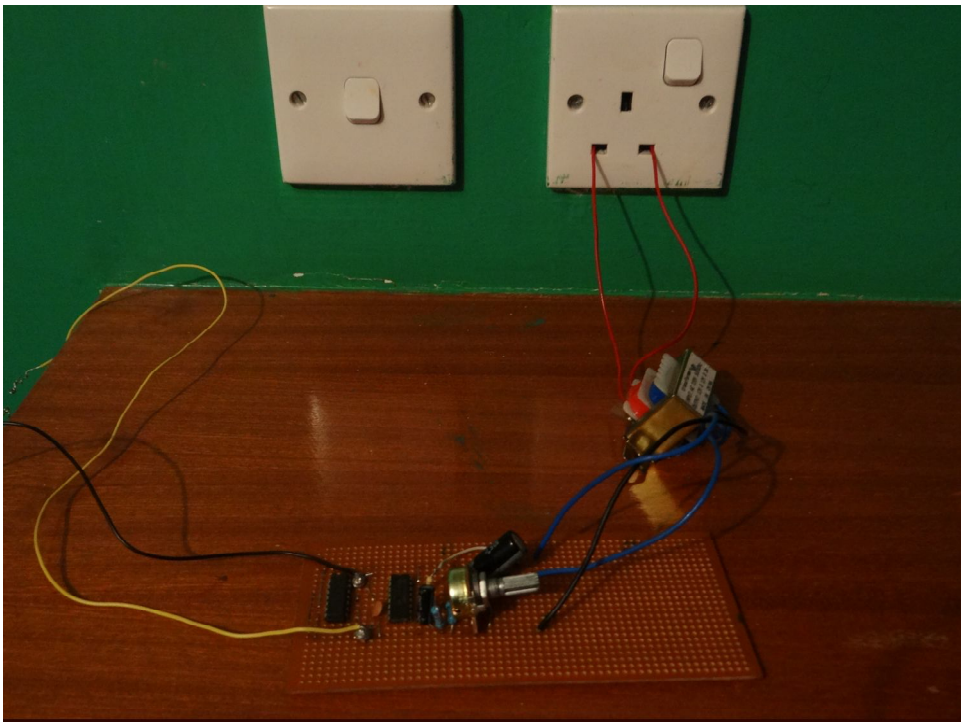


Figure 3.3 Implemented circuit on Proteus



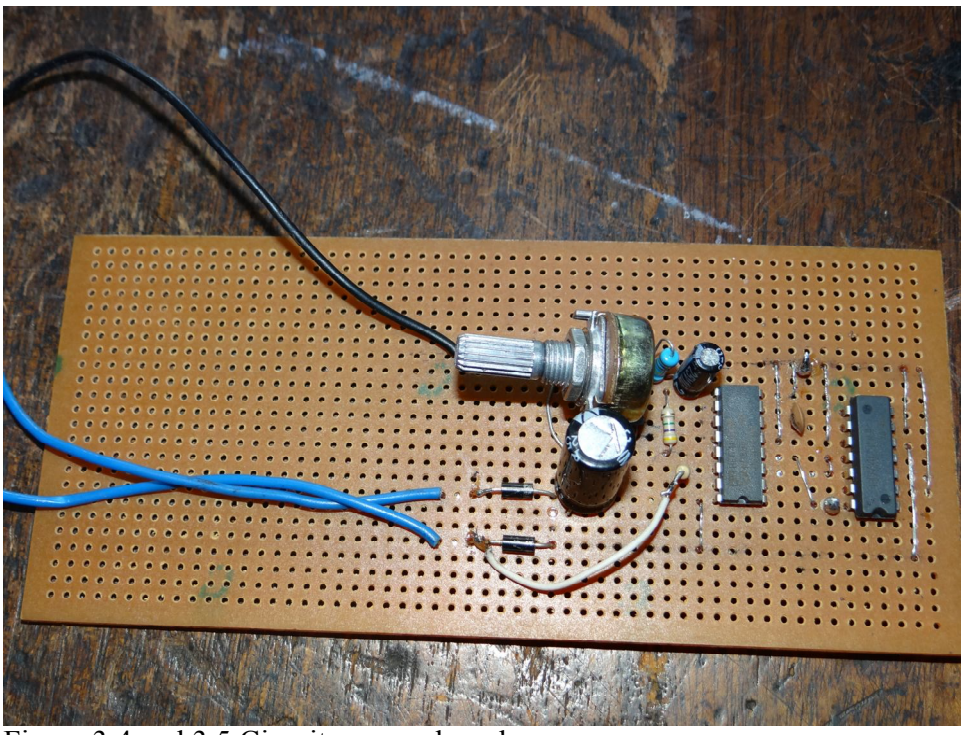


Figure 3.4 and 3.5 Circuit on vero board

3.3 Printed Circuit Board (PCB)

The PCB was used to mechanically support and electrically connect electronic components using conductive tracks, pathways or signal traces etched from copper sheets laminated onto a non-conductive substrate in a process known as fabrication.

i. Fig. 3.6 shows the PCB circuit that was used in the fabrication process.

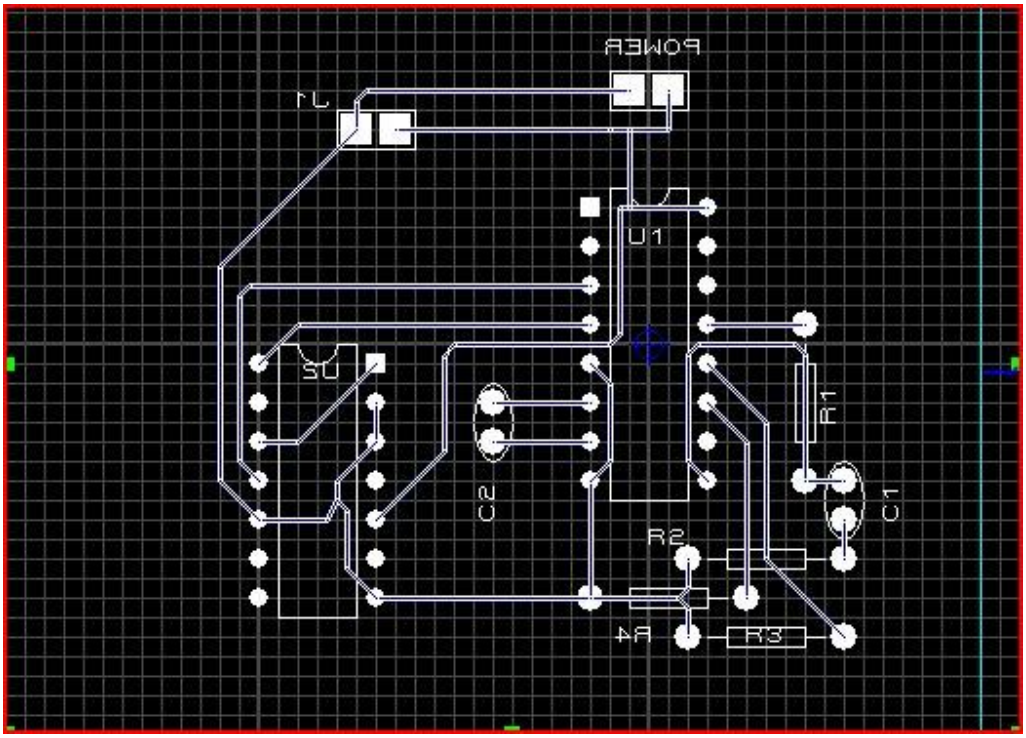


Figure 3.6 : PCB Design

CHAPTER FOUR: RESULTS AND ANALYSIS

4.1 Introduction

This chapter seeks to display the results obtained from the design implementation. The results are divided into two including:

- Simulation results
- Practical results

4.1.1 Software simulation results

The figures 4.1 (a) to 4.1 (e) show the results obtained from simulation using Proteus 8 professional.

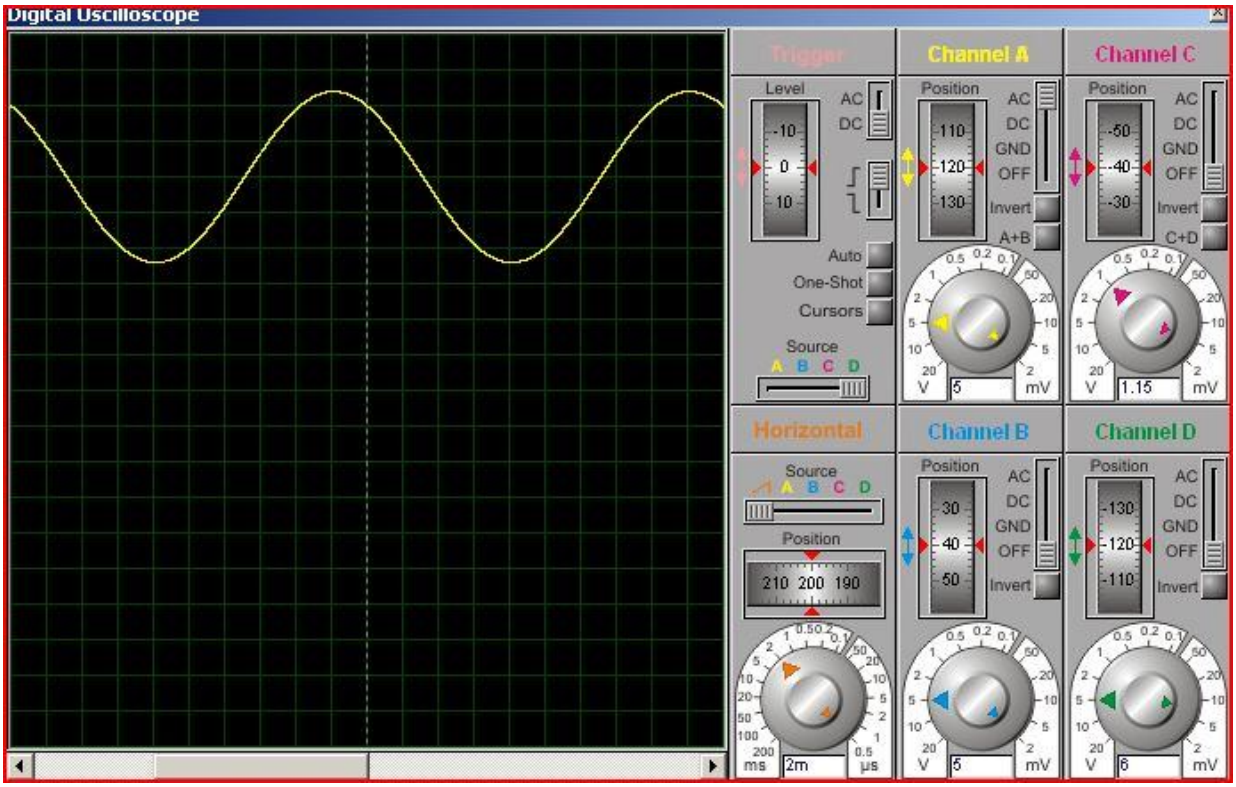


Figure 4.1 (a) The reference input to the phase detector

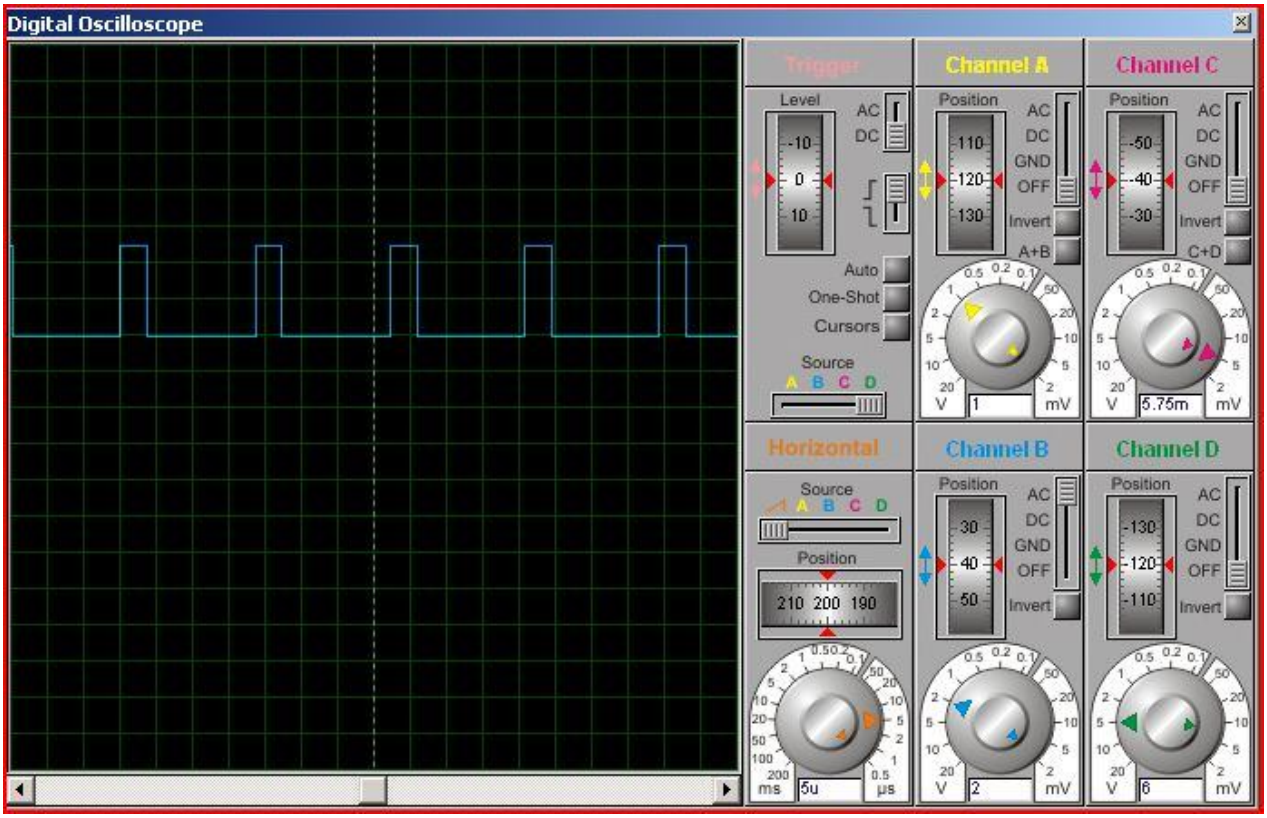


Figure 4.1 (b) The feedback input into the phase detector

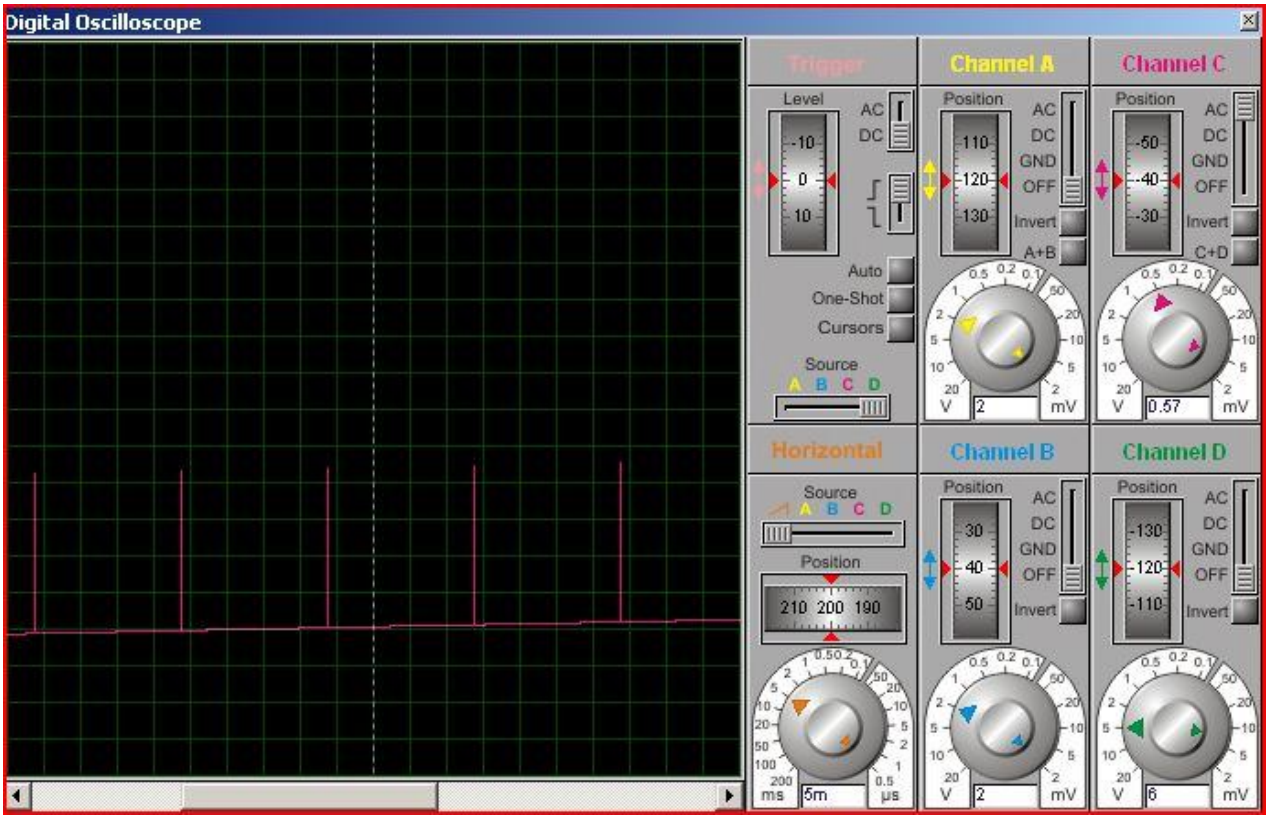


Figure 4.1 (c) Output of the phase detector type II

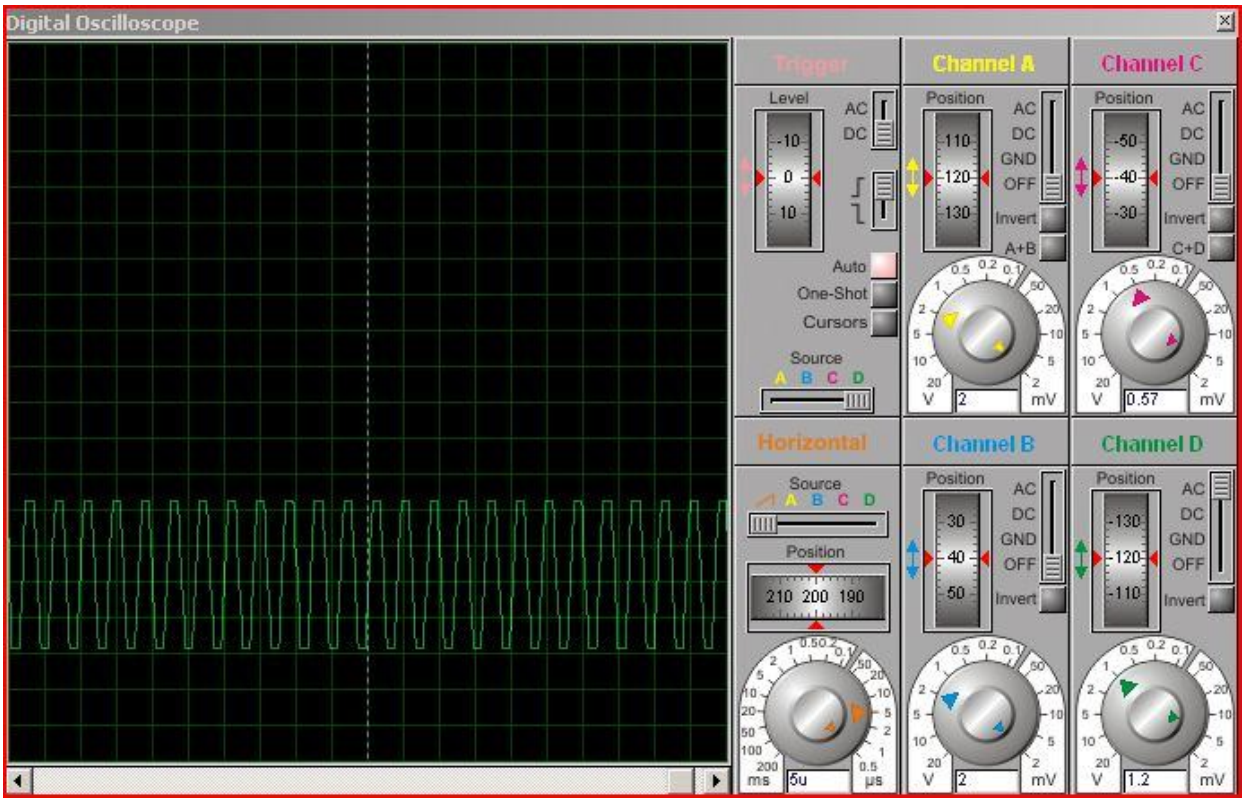


Figure 4.1 (d) Output from the VCO

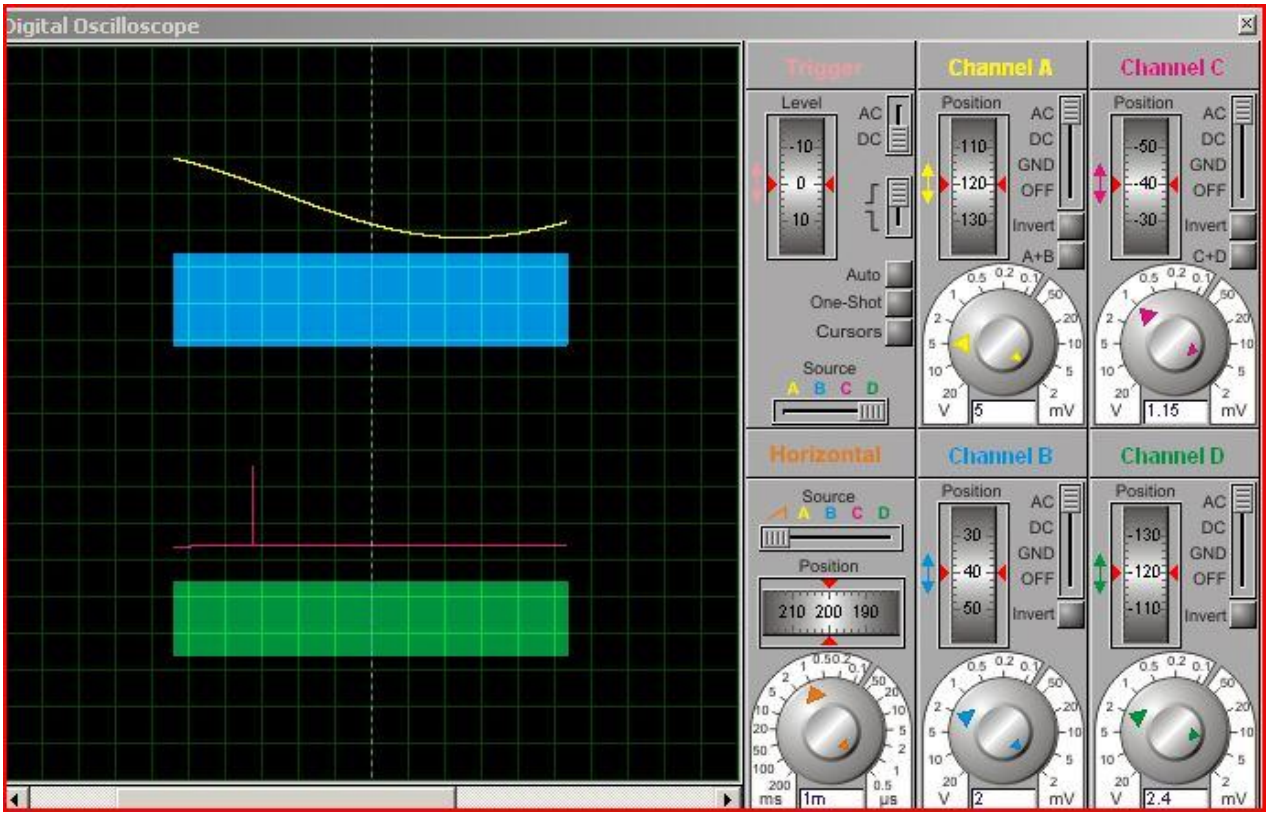


Figure 4.1 (e) A diagram of the inputs into the phase detector and the overall output wave

4.1.2 Practical results

The figures 4.2 (a) and 4.2 (b) show the results obtained from the practical implementation of the designed circuit. The waves show the variation in output frequency when different frequencies are fed back into the phase detector. This shows that the VCO can lock different frequencies provided the frequencies are within its lock range. Beyond this range then the PLL cannot lock.

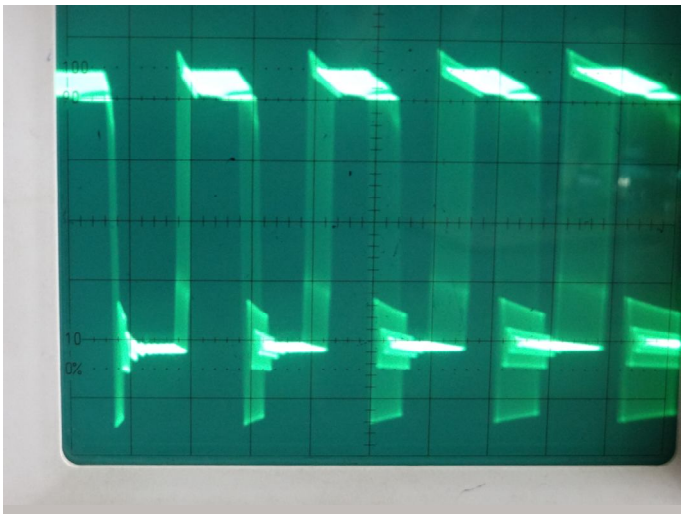


Figure 4.2 (a) Output waveform of VCO of input 50Hz, resistance 253.6 ohms
Time/division 0.5 us/division
Volts/division 2Volts/division

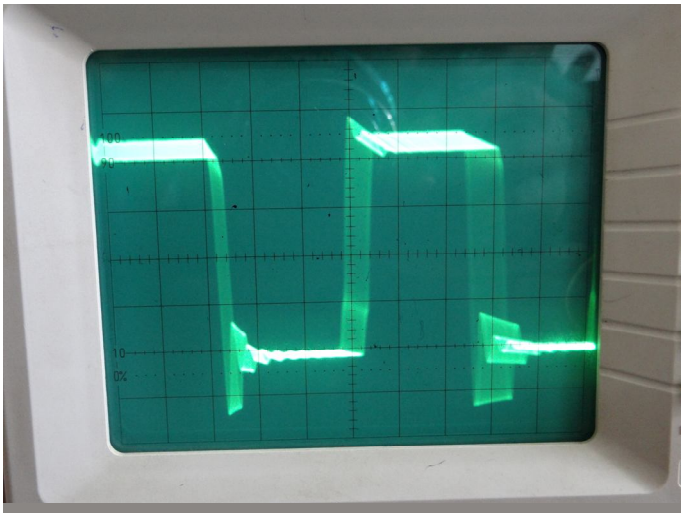


Figure 4.2 (b) Output waveform of VCO of input 50Hz, resistance 253.6 ohms

Time/division 0.2 us/division

Volts/division 2Volts/division

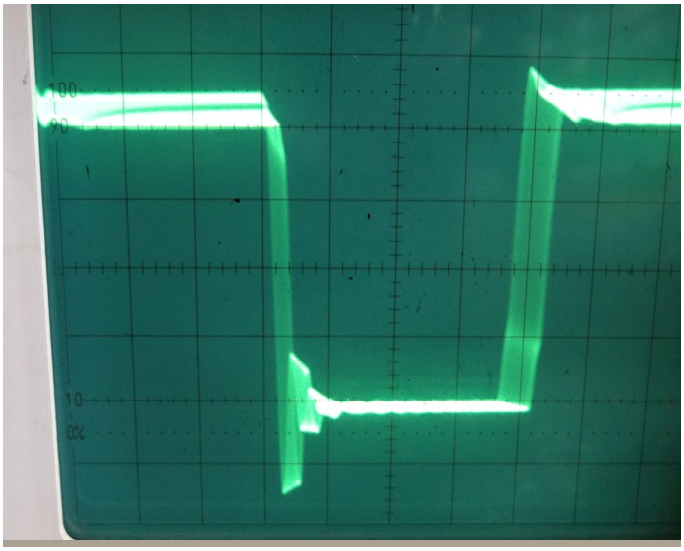


Figure 4.2 (c) Output waveform of VCO of input 50Hz, resistance 4.52 kilohms

Time/division 0.2 us/division

Volts/division 2Volts/division

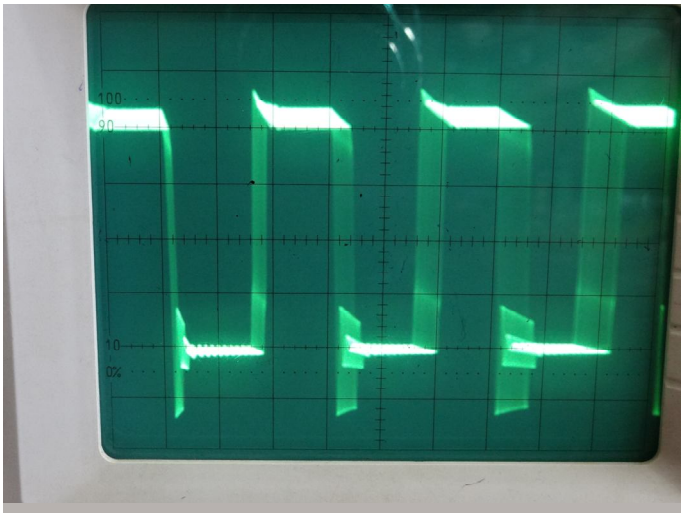


Figure 4.2 (d) Output waveform of VCO of input 50Hz, resistance 4.52 kilohms

Time/division 0.5 us/division

Volts/division 2Volts/division

CHAPTER FIVE: CONCLUSION AND RECOMMENDATIONS

5.1 Discussion

A number of challenges were faced during the implementation of this project. These challenges include:

- Difficult to get the initial desired IC to implement the circuit thus resulting to alternative components in order to make the project a success.

5.2 Conclusion

Phase locked loop remains an interesting topic for the research, as it covers many discipline of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Design with transistors and op amps, Digital circuit design and non- linear analysis.

The objective of this project was reached as it was possible to design a circuit that can generate a multiple of the input signal exploiting the phase locked loop techniques

5.2 Recommendations

The subject of phase locked loop is wide and diverse. There are many other aspects that can be combined in the design to achieve better performance and more powerful systems. For example incorporating a system that can multiply the input frequency with different multiples without having to adjust the calculations.

REFERENCES:

[1] Paul Horowitz. Winfield hill: The Art of Electronics, Second Edition

[2]Amitava Basak. Analogue Electronic Circuits and Systems

[3]Roland Best. Phase-Locked Loops: Design, Simulation and Applications. McGraw Hill, Third edition, 1997.

[4] Robert H. Bishop. Modern Control Systems. Addison Wesley, Seventh edition, 1995.

[5] Gary Miller. Modern Electronic Communication. Prentice Hall, Fifth edition, 1996.

[5] James W. Nilsson. Electric Circuits. Addison Wesley, Fourth edition, 1993.

[6] BehzadRazavi. RF Microelectronics. Prentice Hall, First edition, 1998.

[7] John L. Stensby. Phase-Locked LOOPS: Theory and Application. CRC Press, First edition, 1997.

[8] Neil H. E. weste and Kamran Eshraghian. Principles of CMOS VLSI Design : A System Perspective. Addison Wesley, Second edition, 1992.

[9] Dan Wolaver. Phase-Locked Loop Circuit Design.Prentice Hall, 1991

APPENDIX A: HEF4046B PLL DATASHEET

HEF4046B

Phase-locked loop

Rev. 5 — 18 November 2011 **Product data sheet**

1. General description

The HEF4046B is a phase-locked loop circuit that consists of a linear Voltage Controlled Oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (Zener) diode is provided for supply voltage regulation if necessary. For a functional description see Section 6.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information
All types operate from –40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
HEF4046BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4046BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

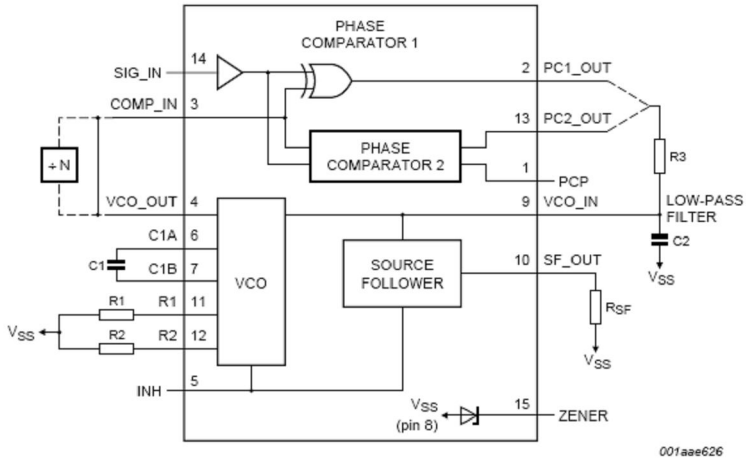


Fig 1. Functional diagram

5. Pinning information

5.1 Pinning

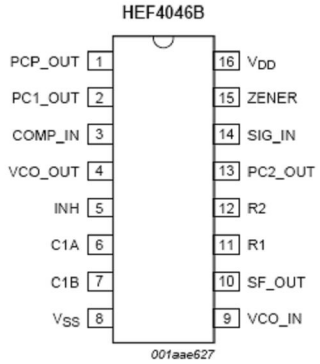


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
PCP_OUT	1	phase comparator pulse output
PC1_OUT	2	phase comparator 1 output
COMP_IN	3	comparator input
VCO_OUT	4	VCO output
INH	5	inhibit input
C1A	6	capacitor C1 connection A
C1B	7	capacitor C1 connection B
V_{SS}	8	ground supply voltage
VCO_IN	9	VCO input
SF_OUT	10	source-follower output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2_OUT	13	phase comparator 2 output
SIG_IN	14	signal input
ZENER	15	Zener diode input for regulated supply
V_{DD}	16	supply voltage

6. Functional description

6.1 VCO control

The VCO requires an external capacitor (C1) and resistor (R1) with an optional resistor (R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO, while resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at SF_OUT (pin 10). If this is used, a load resistor (R_L) should be connected from SF_OUT to V_{SS}; if unused, SF_OUT should be left open. The VCO output (pin 4) can either be connected directly to the comparator input COMP_IN (pin 3) or via a frequency divider. A LOW-level at the inhibit input INH_IN (pin 5) enables the VCO and the source follower, while a HIGH-level turns both off to minimize standby power consumption.

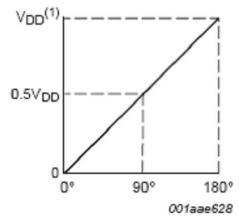
6.2 Phase comparators

The phase-comparator signal input SIG_IN (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input with smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50 % duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to $0.5V_{DD}$ when there is no signal or noise at the signal input. The average voltage to the VCO input VCO_IN is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the center frequency (f_0). The frequency capture range ($2f_C$) is defined as

the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behavior of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center frequency. Another typical behavior is that the phase angle between the signal and comparator input varies between 0° and 180°, and is 90° at the center frequency. Figure 3 shows the typical phase-to-output response characteristic.

Figure 4 shows the typical waveforms for a PLL with a f_0 locked phase comparator 1.



(1) Average output voltage.

Fig 3. Signal-to-comparator inputs phase difference for comparator 1

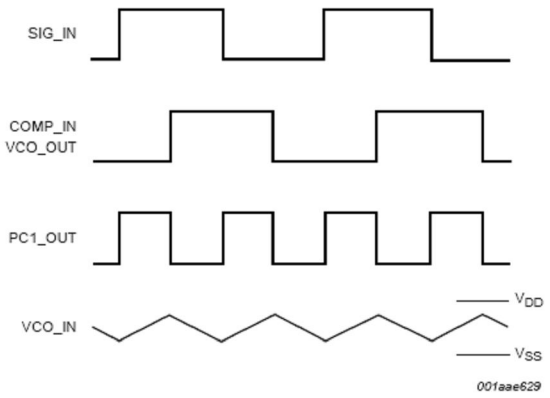


Fig 4. Typical waveforms for phase-locked loop with a f_0 locked phase comparator 1

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers with a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at SIG_IN and COMP_IN. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_OUT) is a HIGH level, which can be used for indicating a locked condition. Thus, for phase comparator 2, no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used, because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2. Figure 5 shows typical waveforms for a PLL employing this type of locked phase comparator.

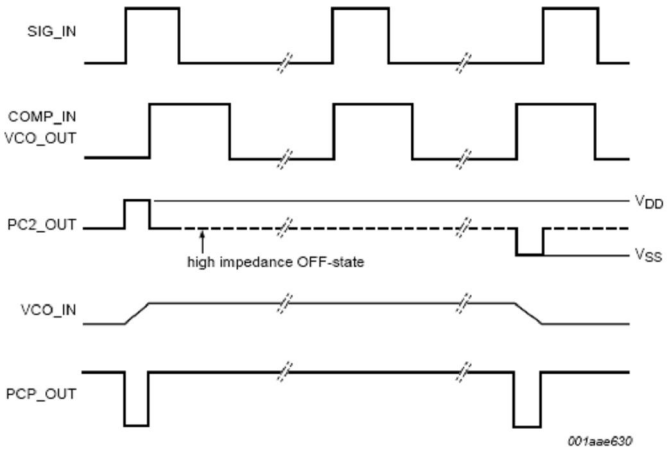


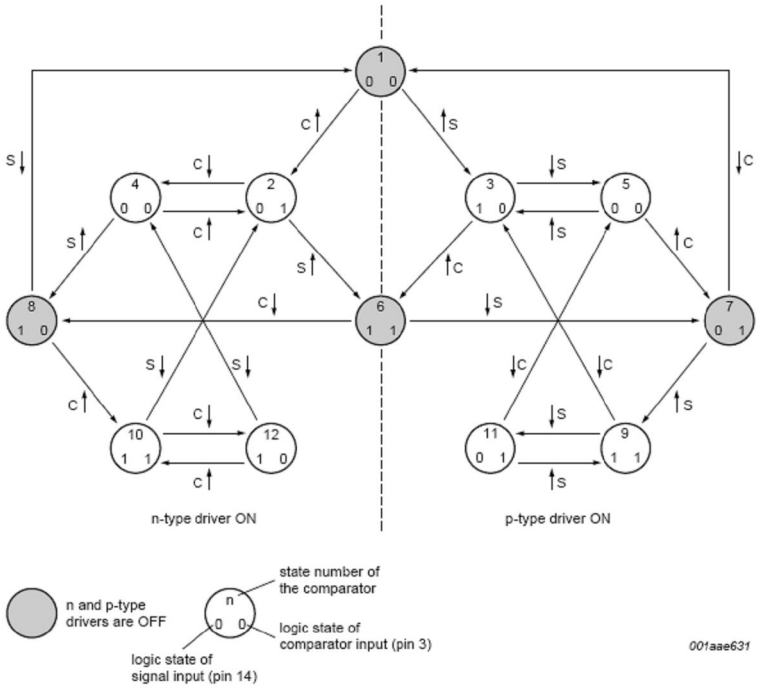
Fig 5. Typical waveforms for phase-locked loop with a locked phase comparator 2

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a '0' for a logic LOW or a '1' for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S representing SIG_IN) or the comparator input (C representing COMP_IN). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes, that only one transition on either the signal input or comparator input occurs at any instant.

- States 3, 5, 9 and 11 represent the output condition when the p-type driver is ON.
- States 2, 4, 10 and 12 determine the condition when the n-type driver is ON.
- States 1, 6, 7 and 8 represent the condition when the output is in its high-impedance OFF state; i.e. both p and n-type drivers are OFF, and the PCP_OUT output is HIGH. The condition at output PCP_OUT for all other states is LOW.



S ↑: 0 to 1 transition at the signal input SIG_IN.

C ↓: 1 to 0 transition at the comparator input COMP_IN.

Fig 6. State diagram for comparator 2

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
		as fixed oscillator only	3	-	15	V
		phase-locked loop operation	5	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	for INH input				
		V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

9. Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
					Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V		3.5	-	3.5	-	3.5	-	V
			10 V		7.0	-	7.0	-	7.0	-	V
			15 V		11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V		-	1.5	-	1.5	-	1.5	V
			10 V		-	3.0	-	3.0	-	3.0	V
			15 V		-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V		4.95	-	4.95	-	4.95	-	V
			10 V		9.95	-	9.95	-	9.95	-	V
			15 V		14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V		-	0.05	-	0.05	-	0.05	V
			10 V		-	0.05	-	0.05	-	0.05	V
			15 V		-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V		-	−1.7	-	−1.4	-	−1.1	mA
		V_O = 4.6 V	5 V		-	−0.52	-	−0.44	-	−0.36	mA
		V_O = 9.5 V	10 V		-	−1.3	-	−1.1	-	−0.9	mA
		V_O = 13.5 V	15 V		-	−3.6	-	−3.0	-	−2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V		0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V		1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V		3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V		-	±0.3	-	±0.3	-	±1.0	µA
I_{OZ}	OFF-state output current	output HIGH and returned to V_{DD}	15 V		-	1.6	-	1.6	-	12.0	µA
		output LOW and returned to V_{SS}	15 V		-	1.6	-	1.6	-	12.0	µA
I_{DD}	supply current		5 V	[1]	-	-	20	-	-	-	µA
			10 V	[1]	-	-	300	-	-	-	µA
			15 V	[1]	-	-	750	-	-	-	µA
		I_O = 0 A	5 V	[2]	-	20	-	20	-	150	µA
			10 V	[2]	-	40	-	40	-	300	µA
			15 V	[2]	-	80	-	80	-	600	µA
C_I	input capacitance	for INH input			-	-	-	7.5	-	-	pF

[1] Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.

[2] Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD};input current pin 14 not included.

10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤20 ns.

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Unit
Phase comparators							
R_I	input resistance	SIG_IN input; at self-bias operating point	5 V	-	750	-	kΩ
			10 V	-	220	-	kΩ
			15 V	-	140	-	kΩ
$V_{i(sens)}$	input voltage sensitivity	SIG_IN input A.C. coupled; peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range	5 V	-	150	-	mV
			10 V	-	150	-	mV
			15 V	-	200	-	mV
V_{IL}	LOW-level input voltage	SIG_IN and COMP_IN inputs, DC coupled LOW; full temperature range	5 V	-	-	1.5	V
			10 V	-	-	3.0	V
			15 V	-	-	4.0	V
V_{IH}	HIGH-level input voltage	SIG_IN and COMP_IN inputs, D.C. coupled HIGH; full temperature range	5 V	3.5	-	-	V
			10 V	7.0	-	-	V
			15 V	11.0	-	-	V
I_{IH}	HIGH-level input current	SIG_IN input; at V_{DD}	5 V	-	7	-	µA
			10 V	-	30	-	µA
			15 V	-	70	-	µA
I_{IL}	LOW-level input current	SIG_IN input; at V_{SS}	5 V	-	−3	-	µA
			10 V	-	−18	-	µA
			15 V	-	−45	-	µA
VCO							
P	power dissipation	f_0 = 10 kHz; R1 = 1 MΩ; R2 = ∞; VCO_IN at 0.5 V_{DD}; see Figure 10 to 12	5 V	-	150	-	µW
			10 V	-	2500	-	µW
			15 V	-	9000	-	µW
f_{max}	maximum frequency	VCO_IN at V_{DD}; R1 = 10 kΩ; R2 = ∞; C1 = 50 pF	5 V	0.5	1.0	-	MHz
			10 V	1.0	2.0	-	MHz
			15 V	1.3	2.7	-	MHz
Δf/ΔT	frequency variation with temperature	no frequency offset (f_{min} = 0 Hz)	5 V	[1] -	0.22 to 0.30	-	% Hz/°C
			10 V	[1] -	0.04 to 0.05	-	% Hz/°C
			15 V	[1] -	0.01 to 0.05	-	% Hz/°C
		with frequency offset (f_{min} > 0 Hz)	5 V	[1] -	0 to 0.22	-	% Hz/°C
			10 V	[1] -	0 to 0.04	-	% Hz/°C
			15 V	[1] -	0 to 0.01	-	% Hz/°C

Table 6. Dynamic characteristics *...continued*

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤20 ns.

Symbol	Parameter	Conditions	V_{DD}		Min	Typ	Max	Unit
Δf/f	relative frequency variation	for VCO see Figure 13 and 14						
		R1 > 10 kΩ	5 V		-	0.50	-	% Hz
		R1 > 400 kΩ	10 V		-	0.25	-	% Hz
		R1 = MΩ	15 V		-	0.25	-	% Hz
δ	duty factor	VCO _OUT output	5 V		-	50	-	%
			10 V		-	50	-	%
			15 V		-	50	-	%
R_{in}	input resistance	for pin VCO_IN				10		MΩ
Source follower								
V_{offset}	offset voltage	R_L = 10 kΩ; VCO_IN at 0.5V_{DD}	5 V	[2]	-	1.7	-	V
			10 V		-	2.0	-	V
			15 V		-	2.1	-	V
		R_L = 50 kΩ; VCO_IN at 0.5V_{DD}	5 V		-	1.5	-	V
			10 V		-	1.7	-	V
			15 V		-	1.8	-	V
Δf/f	relative frequency variation	VCO output; R_L > 50 kΩ; see Figure 13	5 V		-	0.3	-	%
			10 V		-	1.0	-	%
			15 V		-	1.3	-	%
Zener diode								
V_Z	working voltage	I_Z = 50 μA	-		-	7.3	-	V
R_{dyn}	dynamic resistance	For internal Zener diode; I_Z = 1 mA	-		-	25	-	Ω

[1] Over the recommended component range.

[2] The offset voltage is equal to the input voltage on pin VCO_IN minus the output voltage on pin SF_OUT.

11. Design information

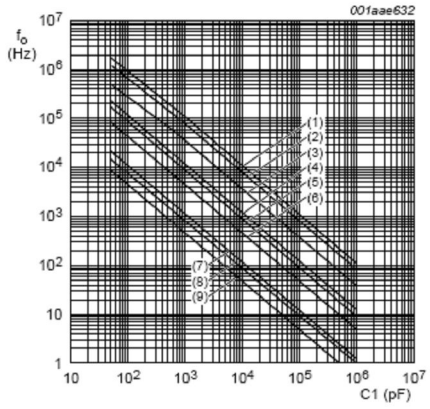
Table 7. Design information

Test	Using phase comparator 1	Using phase comparator 2
VCO adjusts with no signal on SIG_IN	VCO in PLL system adjusts to center frequency (f_0)	VCO in PLL system adjusts to minimum frequency (f_{min})
Phase angle between SIG_IN and COMP_IN	90° at center frequency (f_0), approaching 0° and 180° at the ends of the lock range ($2f_L$)	always 0° in lock (positive-going edges)
Locks on harmonics of center frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range ($2f_L$)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range ($2f_c$)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics; $2f_c < 2f_L$	$2f_c = 2f_L$
Center frequency (f_0)	the frequency of the VCO when VCO_IN at 0.5V_{DD}	

11.1 VCO component selection

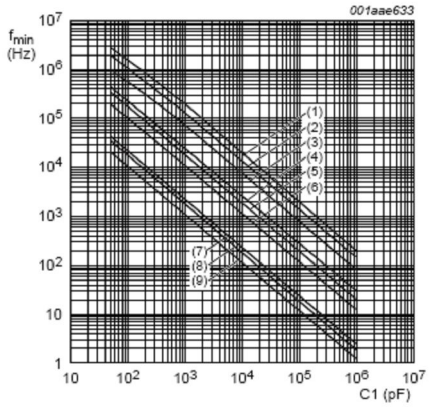
Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞). 0
   a. Given f_0: use f_0 with Figure 7 to determine R1 and C1.
   b. Given f_{max}: calculate f_0 from $f_0 = 0.5 f_{max}$; use f_0 with Figure 7 to determine R1 and C1.
2. VCO with frequency offset.
   a. Given f_0 and $2f_L$: calculate f_{min} from the equation $f_{min} = f_0 - 2f_L$; use f_{min} with Figure 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_0 + 2f_L}{f_0 - 2f_L}$; use $\frac{f_{max}}{f_{min}}$ with Figure 9 to determine the ratio R2/R1 to obtain R1.
   b. Given f_{min} and f_{max}: use f_{min} with Figure 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$ with Figure 9 to determine R2/R1 to obtain R1.



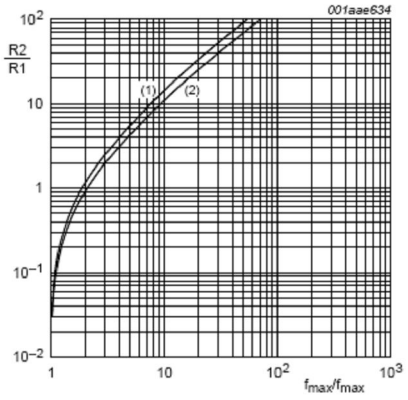
T_{amb} = 25 °C; VCO_IN at 0.5V_{DD}; INH_IN at V_{SS}; R2 = ∞.
Lines (1), (4), and (7): V_{DD} = 15 V;
Lines (2), (5), and (8): V_{DD} = 10 V;
Lines (3), (6), and (9): V_{DD} = 5 V;
Lines (1), (2), and (3): R1 = 10 kΩ;
Lines (4), (5), and (6): R1 = 100 kΩ;
Lines (7), (8), and (9): R1 = 1 MΩ.

Fig 7. Typical center frequency as a function of capacitor C1



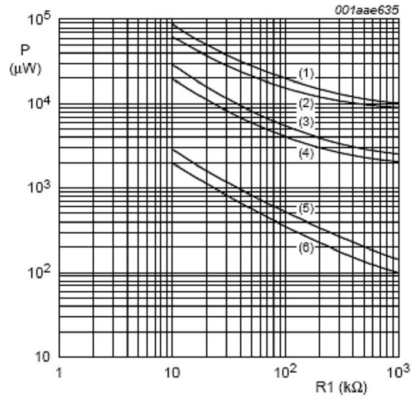
T_{amb} = 25 °C; VCO_IN at V_{SS}; INH_IN at V_{SS}; R1 = ∞.
Lines (1), (4), and (7): V_{DD} = 15 V;
Lines (2), (5), and (8): V_{DD} = 10 V;
Lines (3), (6), and (9): V_{DD} = 5 V;
Lines (1), (2), and (3): R2 = 10 kΩ;
Lines (4), (5), and (6): R2 = 100 kΩ;
Lines (7), (8), and (9): R2 = 1 MΩ.

Fig 8. Typical frequency offset as a function of capacitor C1



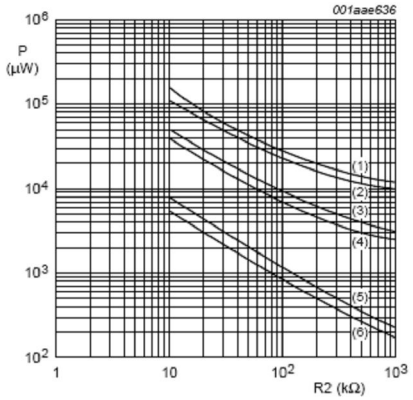
Line (1): V_{DD} = 5 V;
Line (2): V_{DD} = 10 V, 15 V.

Fig 9. Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min}



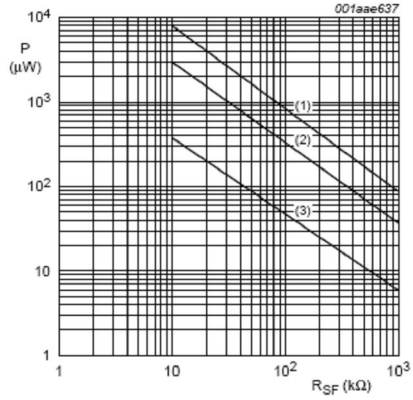
R2 = ∞; VCO_IN at 0.5V_{DD}; C_L = 50 pF.
Lines (1) and (2): V_{DD} = 15 V;
Lines (3) and (4): V_{DD} = 10 V;
Lines (5) and (6): V_{DD} = 5 V;
Lines (1), (3), and (5): C1 = 50 pF;
Lines (2), (4), and (6): C1 = 1 µF.

Fig 10. Power dissipation as a function of R1



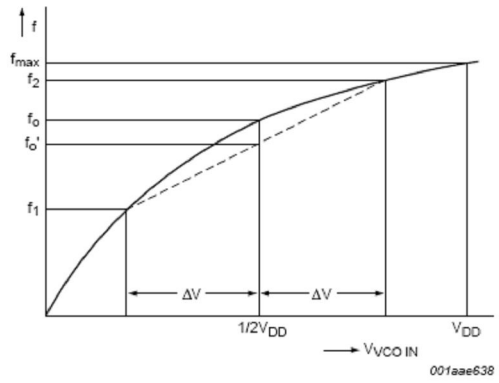
R1 = ∞; VCO_IN at V_{SS} (0 V); C_L = 50 pF.
Lines (1) and (2): V_{DD} = 15 V;
Lines (3) and (4): V_{DD} = 10 V;
Lines (5) and (6): V_{DD} = 5 V;
Lines (1), (3), and (5): C1 = 50 pF;
Lines (2), (4), and (6): C1 = 1 µF.

Fig 11. Power dissipation as a function of R2



VCO_IN at 0.5V_{DD}; R1 = ∞; R2 = ∞.
Line (1): V_{DD} = 15 V;
Line (2): V_{DD} = 10 V;
Line (3): V_{DD} = 5 V.

Fig 12. Power dissipation of source follower as a function of R_L



See Section 10.

For VCO linearity:

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$linearity = \frac{f'_0 - f_0}{f'_0} \times 100\ \%$$

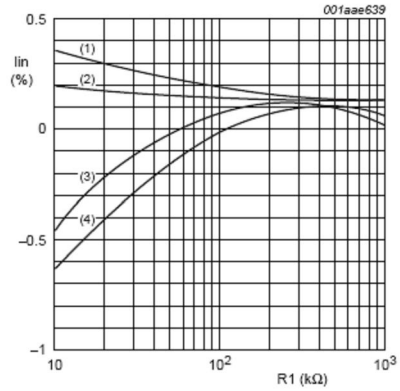
This figure and the above formula also apply to source follower linearity: substitute V_O at SF_OUT for f.

$\Delta V = 0.3$ V at $V_{DD} = 5$ V;

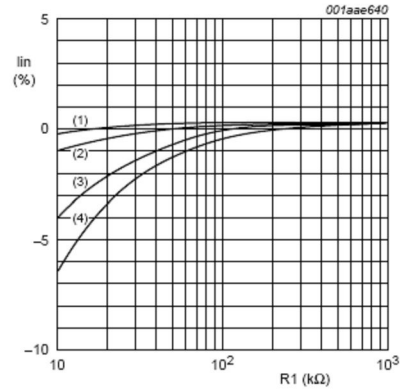
$\Delta V = 2.5$ V at $V_{DD} = 10$ V;

$\Delta V = 5.0$ V at $V_{DD} = 15$ V.

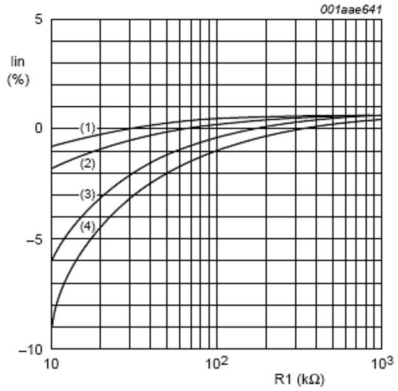
Fig 13. Definition of linearity



a. V_{DD} = 5 V



b. V_{DD} = 10 V



c. V_{DD} = 15 V

R2 = ∞;

Line (1): C1 = 1 μF;

Line (2): C1 = 1 nF;

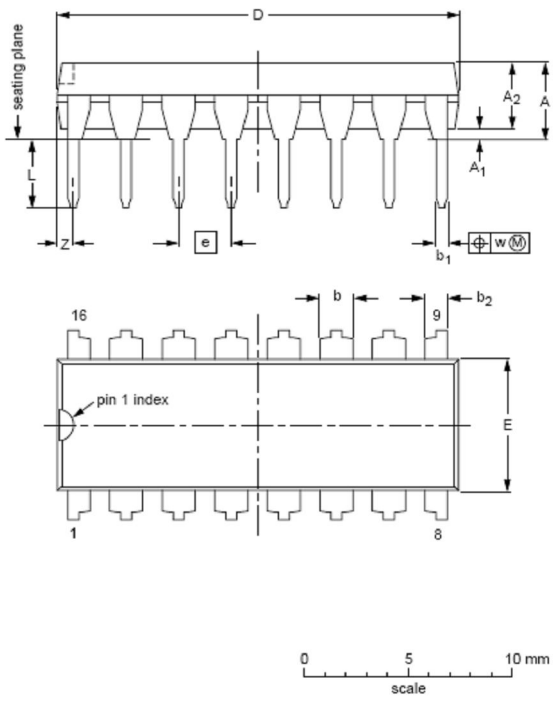
Line (3): C1 = 100 pF;

Line (4): C1 = 50 pF.

Fig 14. VCO frequency linearity as a function of R1

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

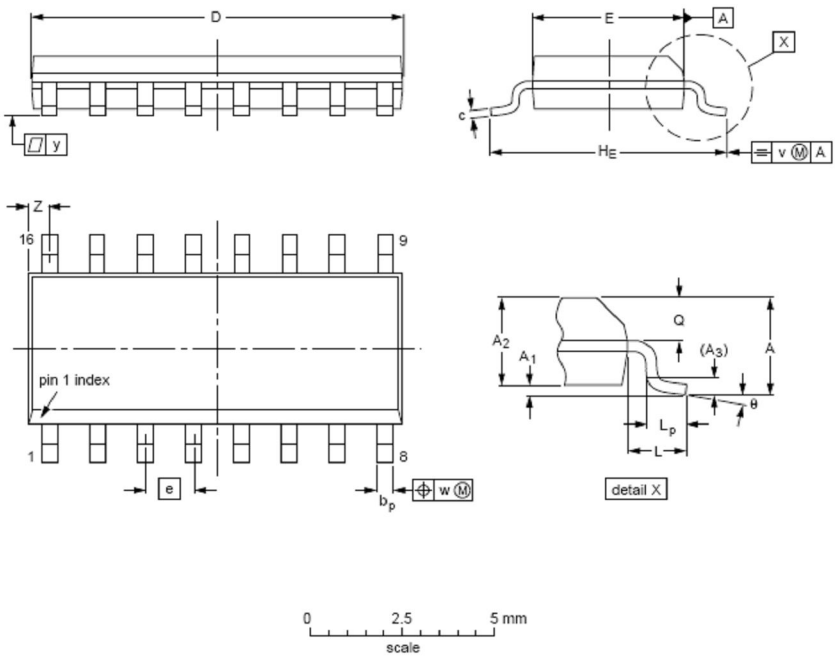
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

13. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4046B v.5	20111118	Product data sheet	-	HEF4046B v.4
Modifications:	• Section Applications removed • Table 5: I_{OH} minimum values changed to maximum • Table 6: R_{in} typical value changed from 10^6 MΩ to 10 MΩ			
HEF4046B v.4	20100105	Product data sheet	-	HEF4046B_CNV v.3
HEF4046B_CNV v.3	19950101	Product specification	-	HEF4046B_CNV v.2
HEF4046B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

14.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

16. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 November 2011

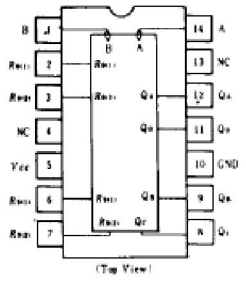
Document identifier: HEF4046B

APPENDIX B: HD74LS90 DECADE COUNTER DATA SHEET

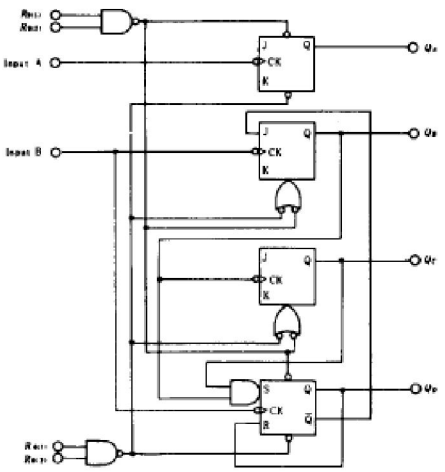
HD74LS90 ●Decade Counters

The HD74LS90 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-five. This device has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications. To use this maximum count length of this counter the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are descrived in the appropriate function table. A symmetrical divide-by-ten count can be obtained from HD-74LS90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7.0	V
Input voltage	R Inputs	V_{IN}	7.0	V
	A, B Inputs		5.5	V
Operating temperature range		T_{opr}	−20 ~ +75	℃
Storage temperature range		T_{stg}	−65 ~ +150	℃

■FUNCTION TABLE

Reset/Count Function Table

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	×	L	L	L	L
H	H	×	L	L	L	L	L
×	×	H	H	H	L	L	H
×	L	×	L	Count			
L	×	L	×	Count			
L	×	×	L	Count			
×	L	L	×	Count			

BCD Count Sequence(Notes1)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary Count Sequence(Notes2)

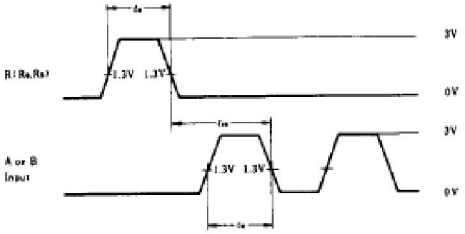
Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes) 1. Output Q_A is connected to input B for BCD count.
2. Output Q_D is connected to input A for Bi-quinary count.
3. H; high level, L; low level, X; irrelevant.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Count frequency	A input	f_{count}	0	–	32	MHz
	B input		0	–	16	
Pulse width	A input	t_w	15	–	–	ns
	B input		30	–	–	
	Reset inputs		15	–	–	
Setup time		t_{su}	25	–	–	ns

■TIMING DEFINITION



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75℃$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$**	–	–	0.4	V
				$I_{OL}=8mA$**	–	–	0.5	
Input current	Any Reset	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	A input				–	–	−2.4	
	B input				–	–	−3.2	
	Any Reset	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	A input				–	–	40	
	B input				–	–	80	
	Any Reset	I_I	$V_{CC}=5.25V$	$V_I=7V$	–	–	0.1	mA
	A input			$V_I=5.5V$	–	–	0.2	
	B input				–	–	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25V$		–	9	15	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan out capability.

*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

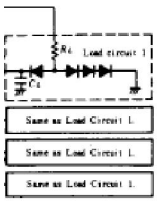
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25℃$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$	32	42	–	MHz
		B	Q_B		16	–	–	
Propagation delay time	t_{PLH}	A	Q_A		–	10	16	ns
	t_{PHL}				–	12	18	
	t_{PLH}	B	Q_D		–	32	48	ns
	t_{PHL}				–	34	50	
	t_{PLH}	B	Q_B		–	10	16	ns
	t_{PHL}				–	14	21	
	t_{PLH}	B	Q_C		–	21	32	ns
	t_{PHL}				–	23	35	
	t_{PLH}	B	Q_D		–	21	32	ns
	t_{PHL}				–	23	35	
	t_{PHL}	Set-to-0	$Q_A \sim Q_D$		–	26	40	ns
	t_{PLH}	Set-to-9	Q_A, Q_D		–	20	30	ns
	t_{PHL}		Q_B, Q_C		–	26	40	

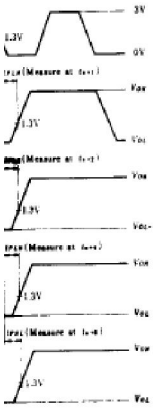
■TESTING METHOD

Item	From input to output	Inputs A	B	R_0	R_9	Outputs Q_A	Q_B	Q_C	Q_D
f_{max}	A→Q	IN	to Q_A	GND	GND	Out	Out	Out	Out
	B→Q	4.5V	IN	GND	GND	–	Out	Out	Out
t_{PLH} t_{PHL}	A→Q_A	IN	to Q_A	GND	GND	Out	–	–	–
	A→Q_D	IN	to Q_A	GND	GND	–	–	–	Out
	B→Q_B	4.5V	IN	GND	GND	–	Out	–	–
	B→Q_C	4.5V	IN	GND	GND	–	–	Out	–
	B→Q_D	4.5V	IN	GND	GND	–	–	–	Out
	R_0^{**}→Q	IN*	to Q_A	IN	GND	Out	Out	Out	Out
	R_9^{**}→Q	IN*	to Q_A	GND	IN	Out	Out	Out	Out

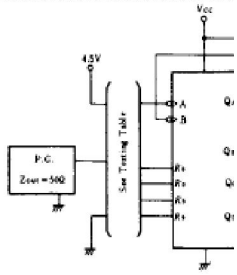
*; For initialized
**; Measured with each input and unused inputs at 4.5V.



$_{HL}$≦6ns,
6
pacitance.

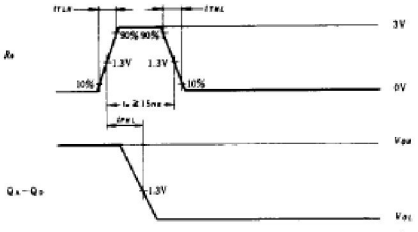


≦5ns, *PRR*=1MHz,
t_{TLH}=t_{THL}≦2.5ns.
outputs are low.

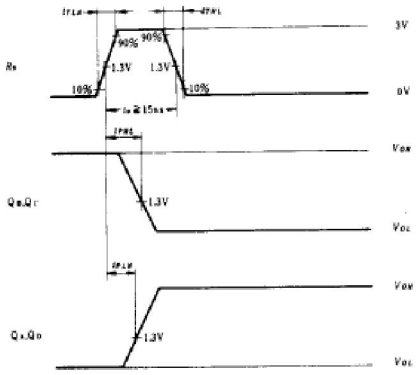


Notes) 1. Input pulse; t_{TLH}≦15
PRR=1MHz, duty cycl
2. C_L includes probe and
3. All diodes are 1S2074

Waveform-2 t_{PHL}(R_0→Q)

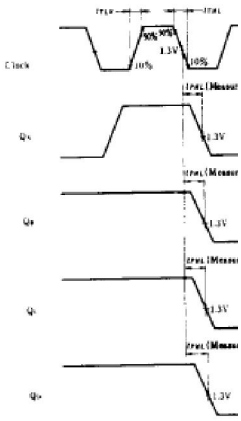


Waveform-3 t_{PLH}, t_{PHL}(R_9→Q)



Notes) 1. t_{TLH}≦15ns, t_{THL}≦5ns.

Waveform-1 f_{max}, t_{PLH}, t_{PHL}(Cloc



Notes) 1. Input pulse; t_{TLH}≦15ns,
duty cycle=50% and: for
2. t_n is reference bit time wi

PACKAGING INFORMATIONS

T-90-2

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

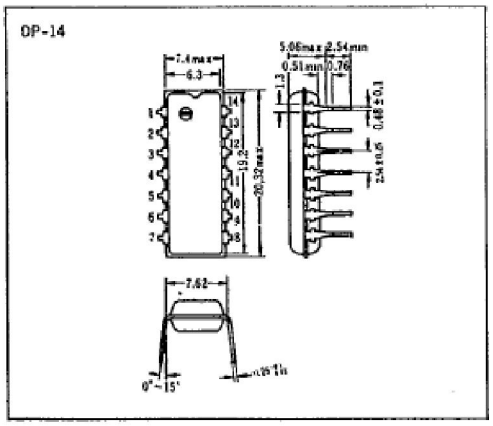
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

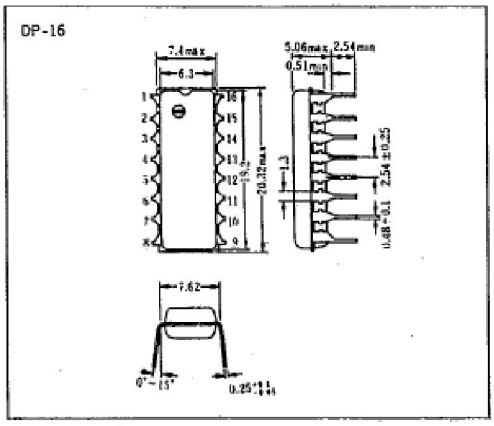
●14 Pin

DP-14



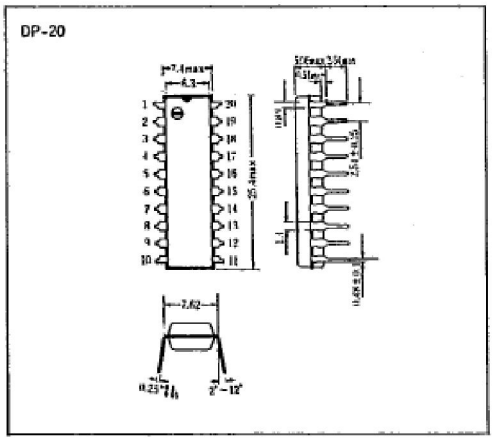
●16 Pin

DP-16



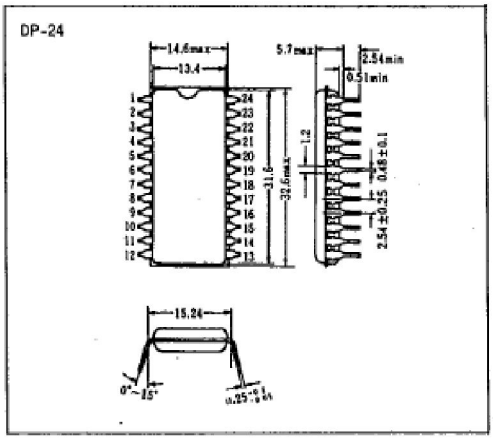
●20 Pin

DP-20



●24 Pin

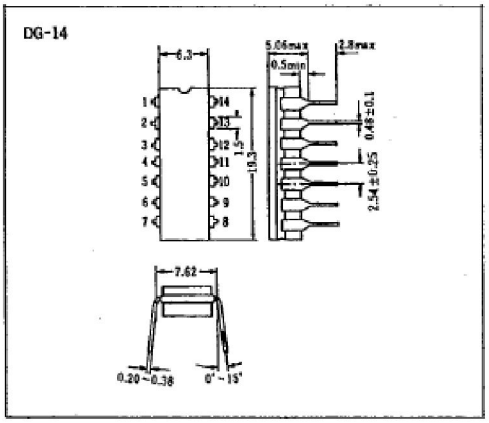
DP-24



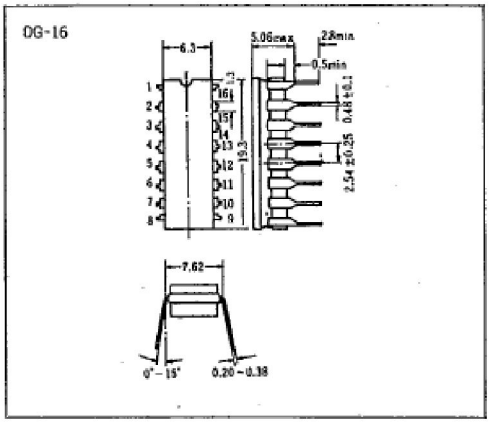
PACKAGING INFORMATIONS

■Cerdip

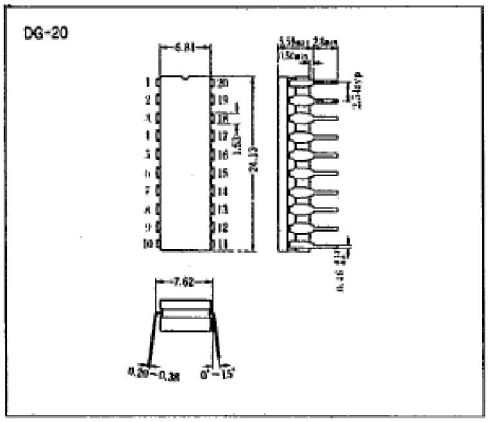
●14 Pin



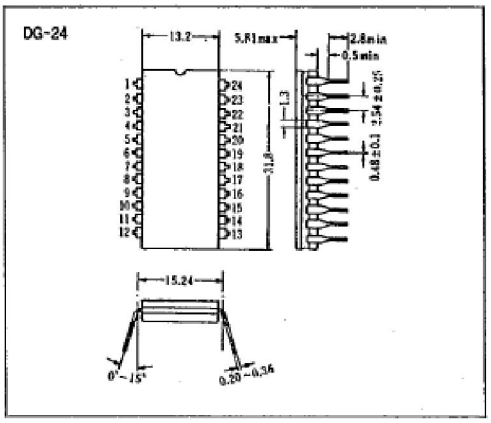
●16 Pin



●20 Pin



●24 Pin



APPENDIX C: COST ANALYSIS

COMPONENT	COST (KSh)
HE4046B	100
HD74LS90	140
VERO BOARD	30
CAPACITORS	40
RESISTORS	30
TOTAL	340